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Microfabrication of a Planar Paul Trap

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Declaration

The work presented in this master thesis was accomplished by the author in Institute for Quantum Information Processing at the University of Ulm, under supervision of Prof. Dr Ferdinand Schmidt-Kaler, from May 2008 to December 2008. The contents are the original work of the author and have not been previously submitted for any other degree or qualification at any academic institution. I hereby declare that I have completed this work independently and using only the aids included. Any passages that have been extracted or cited from other sources have been referenced appropriately.

Ulm, 15.12.2008

Amado Bautista Salvador

I dedicate this thesis to my devoted grandparents Emma and Eliseo Salvador and parents Flavia and Amado Bautista. The persons to whom my heart and life are in debt.

Abstract

The goal of my thesis is the fabrication of a planar complex trapping structure for single ions for applications of quantum information processing. Of high importance is the separation of a trapping device into different regions, either optimized for loading of ions, for their transport, for the manipulation of internal degrees of freedom to realize quantum logic gate operations, for the decoherence free storage of information, and for the readout. Between such regions, we need to shuttle ions and Y-junctions will allow to direct ions either in the one or the other direction as particle beam splitters. The main quest today is to design and fabricate devices which allow for a future scalable quantum processor. A trap design with more than 60 individually addressable DC and RF electrodes has been fabricated. In the focus of this thesis is the application and adaption of microfabrication processing. With a focus on photolithography I have reached an inter-electrode gap with an aspect ratio higher than 1 and inter-electrode gaps of either 1.2 μm, 3.3 μm and 4.8 μm of gold structures on glass substrates. I proved experimentally that these structures sustain electrical breakdown from 180 V for a 1.2 μm inter-electrode gap to 720 V for a 4.8 μm inter-electrode gap. The gold electrodes are plated to a thickness of 6.0 μm.The surface ion trapping device (gap of 4.0 μm) is installed in an ultra high vacuum recipient wired and assembled for single cold ions trapping.

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Introduction

Figure 1: Prehispanic gold ornament

More than one decade ago a quantum computer based on ion trapping in a linear Paul trap and manipulation of the electronic states of the trapped ions (qubits) by laser beams was proposed (1). Experimental and theoretical implements of this original suggestion has demonstrated, during the last years, that it is one of the most promising ways to realize a quantum computer. Most of the requirements for quantum computation (2) have been established in this system, such as efficient quantum state preparation (3; 4; 5), manipulation (5; 6; 7; 8) and read-out (5; 9; 10). Nonetheless the manipulation of a large number of ions in a single trap brings immense technical hindrances to overwhelm. A proposal of an array of microtraps opens up a feasible way to consummate a scalable quantum computer (11). However, the scalability proposals for this system seems to be experimentally complicated to fulfil. Even though, miniaturization of linear Paul traps open the possibility to achieve certain scalability benefits (12; 13), a good quantum networking is not totally accomplished due to the bulky stage of the trap design that normally do not allow interconnection within single traps.

In this context, a new architecture in the ion trapping proposal should be sought in order to bring the desired scalability. In recent years, a new bid, a geometry modification of the linear Paul trap by lying the trapping electrodes in

a single plane appear as the most promising candidate (14). In addition to cover up the scalability pothole, it also commends the possibility of the construction of reliable quantum networking. It is expected, in few years, that manipulation and transport (15) of large number of atoms trough T-junctions (16) and Y-junctions (17) to be implemented. Moreover, straightforward fabrication procedures such as photolitography and metal deposition may be elaborated to execute such planar ion traps (14; 18).

The advantages of this new trap design, so far, are diverse. Among the most remarkable stand out the device miniaturization, the feasible quantum networking with the help of T- and Y-junction, the suppression of heating rates under cryogenic environments (18), and the increment of optical access compared to traditional Paul traps (19).

In this respect, this thesis contributes to the rapid and challenging experimental development of the surface-electrode architecture. Under this purpose, the fabrication of a gold five-wire surface-electrode trap with the smallest inter-electrode gaps and high inter-electrode aspect ratio reported in the literature is revealed. Specifically, the smallest inter-electrode gap achieved in this work has a value of 1.2 μm, which sustained an average electrical breakdown about 182.3 V in DC mode. These fascinating realizations are accomplished by utilizing photolithography, electroplating and etching as main processing steps.

This master thesis is divided in the following way. In the Chapter 1 the formalism of trapping potentials for an ideal Paul trap is developed as well as the trap design parameters. The succeeding chapter 2 is an overview of the lithography, deposition and etching processes which form the pillars of the whole fabrication procedure towards the final acquisition of our designed surface-electrode trap. Chapter 3 justifies the fabrication layout with few comparisons, underlying advantages of the materials employed so as to achieve our desired trap. The whole experimental work, results, and discussion encountered during the progress of this thesis is fully described in the chapter 4. A final chapter 5 includes electrical breakdown results of succeeding trap chips with 1.2 μm and 4.8 μm inter-electrode gaps.

Chapter 1

Paul Traps

> *The difficulty of literature is not to write, but to write what you mean; not to affect your reader, but to affect him precisely as you wish.*
>
> Robert Louis Stevenson

Paul traps have been useful as an universal tool to hold charged particles, their applications reach from chemistry and mass spectroscopy, to quantum optics and quantum information. Wolfgang Paul invested the principle in 1958 and he was rewarded the Nobel prize in 1989 when the importance of this invention had become clear. This chapter is dedicated to the explanation of the principles of dynamical confinement. We start out with a 3D Paul trap, continue to planar Paul traps, and then segmentation of Paul traps, leading finally to explain the specific planar segmented which is used in this experiment. At the end of this chapter a detail explanation of the mask design for its fabrication is provided.

1.1 Paul Trap

To understand trapping and manipulation of ions one has to describe the trapping electric potentials involved in an ion trap as a first step. We require for the experiments a harmonic potential with a linear restoring force that drives any charged particle with mass m back into the very center of the trap. As the force

is the gradient of the electric potential, this requires a quadratic potential shape of the form

$$\Phi(\mathbf{r}) = \Phi_0 \sum_i \alpha_i (r_i/\tilde{r})^2 \quad , \quad i = x, y, z \tag{1.1}$$

This sort of potential may be formed by well suited electrodes around which are supplied with an electric voltage. Any electric field has to fulfill Maxwell's equations, more specifically the Laplace equation which reads for the free space with a charge density equals zero. The Laplace condition $\Delta\Phi = 0$, demands

$$\alpha_x + \alpha_y + \alpha_z = 0. \tag{1.2}$$

We see that harmonic confinement in two axes, say x and y leads to a negative coefficient in z, thus anti-confinement. Wolfgang Pauls solution was the introduction of a time dependent driving field $\Phi(t)$.

$$\Phi_0(t) = U + V cos(\Omega_{RF} t) \tag{1.3}$$

with a static part U and a dynamic part V that oscillates at the frequency $\Omega_{RF}/2p$.

The dynamic stabilization can be exemplified by a mechanical analogue device (20), as depicted in Figure 1.1. It consists of a small steel sphere situated in the saddle point of a surface. The unstable point is encountered when the device is held static, since the steel ball merely will roll off the surface. On the contrary, if the surface is swiveled with a convenient angular frequency around the normal axis, the small ball will stay rounding around the the rotation axis of the surface potential for a long time.

To describe the behavior of a trapped ion in such a saddle curve, one takes into account the equations of motion of a particle carrying a charge Q and a mass m.

$$\ddot{r_i} + \frac{2\alpha_i Q}{m\tilde{r}^2}(U + V\cos(\Omega_{RF} t))r_i = 0 \tag{1.4}$$

and they may be rewritten in the canonical form of the Mathieu equation

$$\frac{d^2u}{d\tau^2} + (a - 2q\cos(2\tau))u = 0 \tag{1.5}$$

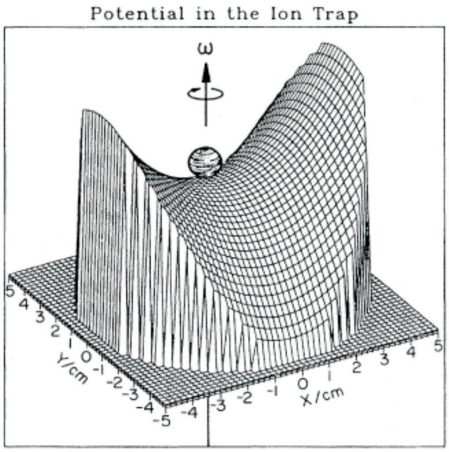


Figure 1.1: Mechanical analogue (20)

with the substitutions

$$a_i = -\frac{8\alpha_i QU}{m\tilde{r}^2{\Omega_{RF}}^2} \tag{1.6}$$

$$q_i = \frac{4\alpha_i QV}{m\tilde{r}^2{\Omega_{RF}}^2} \tag{1.7}$$

and $\tau = \frac{1}{2}\Omega_{RF}t$. Moreover, the stable solutions of the Mathieu equation can be expressed in the form of a Fourier series (21), thus

$$u_j(\tau) = A_j \sum_{n=-\infty}^{+\infty} c_{2n}\cos[(\beta_j + 2n)\tau] + B_j \sum_{n=-\infty}^{+\infty} c_{2n}\sin[(\beta_j + 2n)\tau], \tag{1.8}$$

where A_j and B_j are constants depending on the initial conditions. The trajectory of a particle $u(\tau)$ undergoes oscillations which show both frequencies, the driven motion, also called micro motion at frequency $\Omega_{RF}/2p$ and the secular motion at frequency $\Omega_{RF}/2p$. For the coefficients c_{2n}, which are the amplitudes of the Fourier components of the particle motion, we have the succeeding recursion formula:

$$\frac{c_{2n}, j}{c_{2n\mp 2}, j} = -\frac{q_j}{(2n+\beta_j)^2 - a_j - \frac{q_j^2}{(2n\pm 2+\beta_j)^2 - a_j - \ldots}} \tag{1.9}$$

For the stability parameter β one obtains a continued fraction expression:

$$\beta_j^2 = a_j + f_j(\beta_j) + f_j(-\beta_j), \quad f_j(\beta_j) = \cfrac{q_j^2}{(2+\beta_j)^2 - a_j - \cfrac{q_j^2}{(2n\pm+\beta_j)^2 - a_j - \ldots}} \tag{1.10}$$

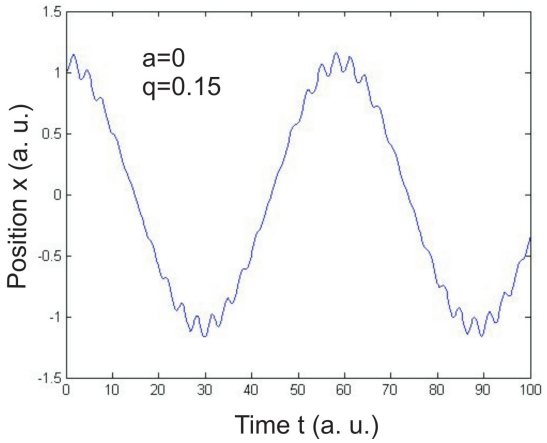


Figure 1.2: Both frequencies components are visible the secular slow and the superimposed micromotion.

When the trajectories of the charged particles are bounded in all directions a stable trapping of ions is possible. What is more, we realize from Eq. 1.10 that the value β and as consequence the stability or instability of the solutions depends only on the parameters a and q. Thus the region of stable trapping parameters is obtained by overlaying the stability diagrams for motion in all three directions, as bared in Figure 1.3a. If the quadrupole potential is rotationally invariant about the z axis, the stability parameters a_i, q_i are given by

$$a_x = a_y = -\frac{8QU}{m({r_0}^2 + 2{z_0}^2){\Omega_{RF}}^2} \qquad a_z = -2a_x \tag{1.11}$$

$$q_x = q_y = \frac{4QV}{m({r_0}^2 + 2{z_0}^2){\Omega_{RF}}^2} \qquad q_z = -2q_x\,, \tag{1.12}$$

where $\alpha_x = \alpha_y = 1$, $\alpha_z = -2$ and $\tilde{r}^2 = {r_0}^2 + 2{z_0}^2$ are setting for a 3D trap. This choice ensures that $\Phi(r_0, 0, 0, t) - \Phi(0, 0, z, t) = U + V\cos(\Omega_{RF}t)$.

There is an important region for practical purposes, so to speak, the lowest stability domain which is the region near the origin. The traps required for

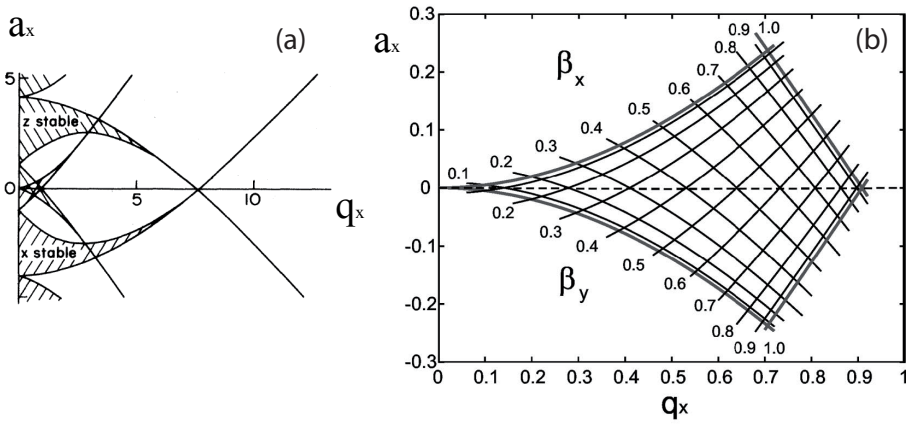


Figure 1.3: Stability domains for a) the ideal 3D Paul trap and b) the lowest stability diagram of a linear RF trap. Taken from (22)

ion confinement work in this lowest region. The shape of the stability diagram depends on the real parameters of Eq. 1.1.

A useful trap electrode configuration is that for the linear RF trap. For this trap the parameters are related as

$$a_z = 0, \quad a_y = -a_x \tag{1.13}$$

which leads to

$$q_y = -q_x, \quad q_z = 0. \tag{1.14}$$

Particularly, the first stability region is symmetric around q_x axis, since the borderlines of stability in the two directions are mirror images of each other, as shown in Figure 1.3b.

This configuration encompasses four parallel linear electrodes, each of them facing each other and equidistant from trap axis. As we can realize from Figure 1.4, two of these electrodes, in opposite positions about the trap axis, are driven by RF potential, whereas the other two "control" electrodes are sustained at DC potential. This configuration allows the creation of the required quadrupolar RF field for ponderomotive confinement in the lateral directions. The two control electrodes are segmented along their own axis, and static potentials are applied

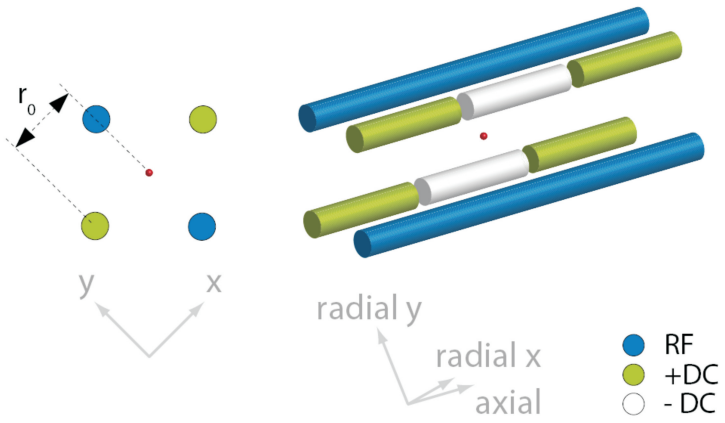


Figure 1.4: Standard four-rod, linear RF trap. Taken from (22)

to the sections to create longitudinal confinement (14). The focus of next section is related to a planar modification of the previously discussed linear trap.

1.2 Surface-Electrode Ion Trap

Another type of Paul trap where the configuration of electrodes lying on a single plane may be viable by deformation of linear Paul trap is presented in this section. This deformation of quadrupolar linear geometry into a plane conserves the quadrupolar potential for ion confinement. At the same time, it allows us the fabrication of smaller devices, by conventional fabrication processing such as photolithography since the whole structures lie on a unique plane (14).

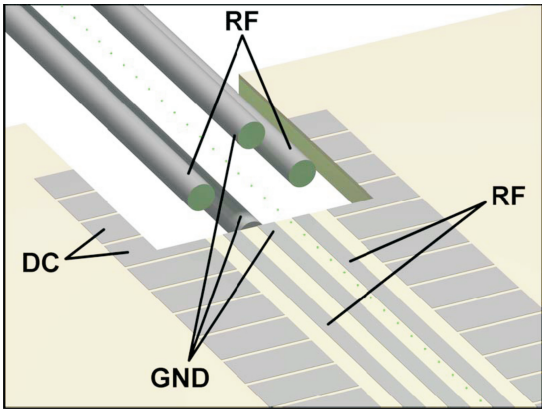


Figure 1.5: Deformation of linear RF into surface-electrode trap. Taken from (23)

An immediate planar geometry

that might come out from Figure 1.4, resides in the fact to alternate one control electrode and one RF electrode into a plane such that the final arrangement (RF, control, RF, and control) is a *four-wire* layout as displayed in Figure 1.6a. This kind of assembly seems to be promising but implicates a more elaborate fabrication processing, due to the need of electrical supply to control electrodes. Therefore, these contacts must be done either by building up multi layered structures or construction of vias through the substrate. Although segmentation of outer RF and control electrodes are feasible and different control potentials might be applied, this is difficult to complete due to the difficulty of applying control potentials to the electrodes without altering application to RF electrodes (14). Another possibility is an axial constriction via the segmentation of the outer control electrode. Nevertheless, a compensation from other non-segmented control electrode is mandatory to compensate for the lateral field due to the single segmented electrode. As consequence the fabrication of T-junctions with four-wires configuration might be difficult.

(a) Four-wire geometry (b) Five-wire geometry

Figure 1.6: Possible configurations for surface-electrode trap. Modified from (14)

A geometry that surpasses these complications may be implemented by designing a *fire-wire* configuration, in which the center and outer electrodes are sustained to RF ground, and the rest of electrodes to RF potentials, as disclosed in Figure 1.6b. In this array, the trap axis is situated above (and below) the central electrode, and the outer electrodes may be segmented for longitudinal confinement and control (14). An interesting possibility appear promising if the center electrode may be segmented. However, same complications explained before where the need of connections to inner electrodes bring out more complicated fabrication processing. Due to the mirror-like symmetry in the middle of inner RF ground electrode, the five-wire design permits the reliable construction of

T-junctions (14), straight and modified X-junctions (23) as well as Y-junctions (17), as it is in our case.

Analytical Approach

Typically, the estimations for the electrical potential in the surface-electrode geometry are done numerically (23; 24). There exist analytical solutions to Laplace equation when appropriate boundary conditions are applied. In those cases, the design parameters of a surface-electrode ion trap may be studied either in 2D (15) or 3D space (19) for high symmetry designs. We have developed a numerical toolbox to calculate numerically the static and dynamic confinement of trapped particles.

1.3 Trap Design

RF electrode design

Our surface-electrode trap design obeys the five-wire geometry discussed in previous section. The RF electrodes create a local minimum in the absolute value of the electric field above the electrode surface, as it is analytically suggested (19). The RF electrode arrengement is drawn in Figure 1.7, where the designed two RF electrodes (gray color) are considered to be infinitely long in the z dimension. One electrode has edges at $x = -c$ and $x = 0$, whereas the other has edges at $x = a$ and $x = a + b$. The voltages applied to the electrode surface $y = 0$ are

$$\phi(x,0,t) = \begin{cases} 0, & x < -c, \\ V_{RF}\cos(\Omega t), & -c < x < 0, \\ 0, & 0 < x < a, \\ V_{RF}\cos(\Omega t), & a < x < a + b, \\ 0, & x > a + b. \end{cases} \tag{1.15}$$

Where V_{RF} potential represents the peak voltage applied to the RF electrodes and Ω is the RF angular frequency. The dimensions of the electrodes are described by the parameters a, b and c and they are measured from the center of the gap instead of the corresponding edges.

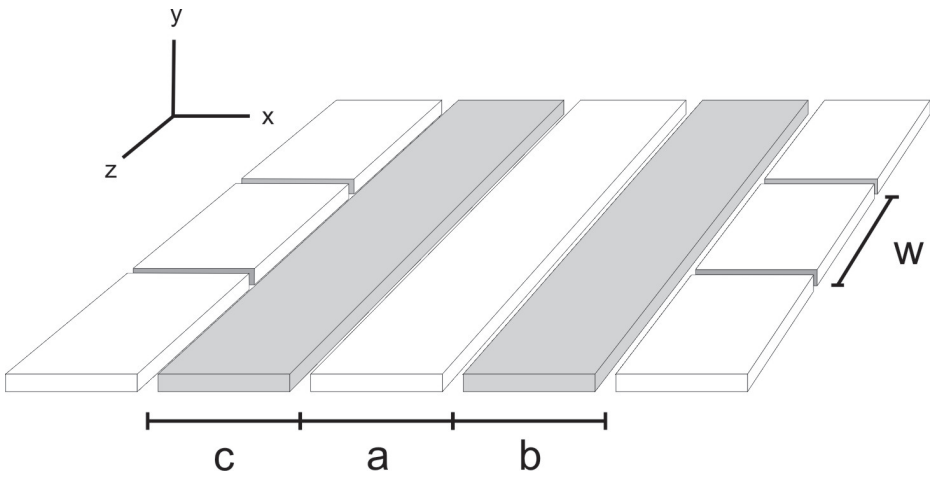


Figure 1.7: Surface-electrode trap design

We follow the 3D approach (19) and it turns out that, the trap center is at $x_0 = a/2$, $y_0 = \sqrt{2ab + a^2/2}$. The escape point of the trap can be found to be situated at $x_e = a/2$, $y_e = \sqrt{2ab + a^2 + 2(a+b)\sqrt{2ab + a^2/2}}$. Evaluating this point at the pseudopotential one determines the trap depth (19) as

$$\psi_e = \frac{Q^2 V_{RF}}{\pi^2 m \Omega^2} \left[\frac{b}{(a+b)^2 + (a+b)\sqrt{2ab + a^2}} \right]^2 . \tag{1.16}$$

We can observe the pseudopotential plot, as displayed in Figure 1.8, and realize there is a point that interconnects the trap center region with the region where the potential diminishes to zero as $y \to \infty$ (19). This is a saddle point above the trap that corresponds to the lowest potential. Therefore it represents the easiest point where an ion trapped inside the pseudopotential well can escape from the trap. The best estimation of the depth of the trap is encountered at this *escape point* since it represents the maximum energy at which an ion can be contained by the trap. There is no general analytical solutions to this point except for the four and five-wire geometries. For different geometries as previously discussed numerically estimations have been used.

In a typical situation of a planar trap with dimensions of about 100 to 200 μm, a potential depth of the order of 100 mK is reached

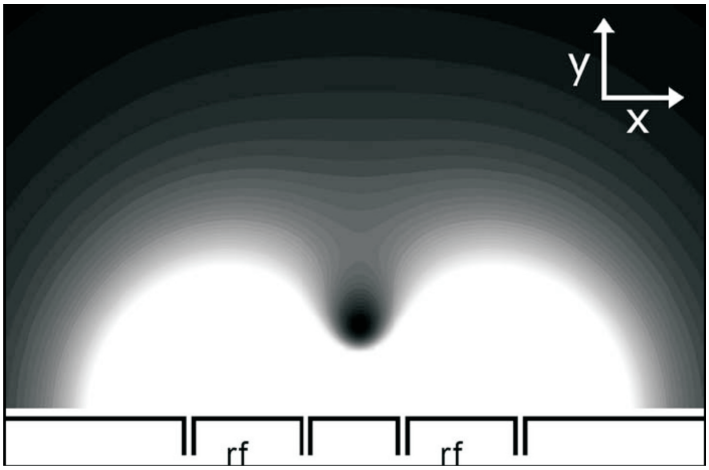


Figure 1.8: Psuedopotential well produced above surface electrodes by the electrical field resulting from the five-wire configuration. Dark regions correspond to low pseudopotential energy. The ion is trapped on the center of the trap, the dark region near the center of picture, and the maximum energy the ion can have and be trapped is given by the difference between the center of the trap and the saddle point. Taken from (19)

Control electrode design

As it has been explained before the RF electrodes allow confinement in the xy plane, whereas in the z dimension the ion is trapped by a static potential. From the surface-electrode design shown in Figure 1.7, we have chosen a segmentation of the outer RF ground electrodes, with the intention that alternating voltages produce a static potential that is trapping in z dimension. In this way, the position of the center of the trap can be varied in the z direction by changing the voltages applied. In addition, it permits to adapt, in a controlled way, the minimum of the ions potential well along z direction of the trap (15).

Analytical results from 3D approach state that when the five-wire geometry and a ratio $b/a = 1.2$ are chosen a good value for the control electrode width is $w \approx 4a$. This is due to the fact that the width of the control electrodes should be chosen in such a way that the field it creates has significant curvature everywhere along the path of the ion near the electrode (19).

Chapter 2

Principles of Microprocessing

The true work of art is but a shadow of the divine perfection.

Michelangelo

This chapter includes an overview of the main processes used during chip fabrication. At first, a brief discussion about photolitography is presented. In a second section, two deposition processes, thermal evaporation and electroplating, are explicated. In the final section, the basics of wet and dry etching are treated.

2.1 Lithography

Modern lithography [1] does move away from ancient lithography, where pattern on stony or metallic surfaces were created by applying mechanical or chemical means. Indeed, modern lithography is an etching process where those bulky surfaces have been substituted by chemicals or organic polymers, *resists*, containing a photoactive compound and by an electromagnetic wave source which play the role of the writing source. Basically, depending on the type of source and the resist sensitivity, the lithography has an specific application as well as a special name. As some examples we find electron beam (e-beam) lithography, x-ray lithography and optical lithography (photolithography), among others.

[1] By this term we do refer to patterning of electronic devices at micro and nano scales, and in this work will be refereed in the future only as lithography

Mainly, to achieve a lithography process one requires: i) a source, ii) a mask, which is a replica of the intended structure, iii) a resist, chemically sensitive to the source, and iv) a developer, which plays a similar role like in photography revealing exposing parts of the resist. In the next section the mask fabrication procedure is explained.

2.1.1 Optical Lithography

Optical lithography (photolithography) refers to a lithographic process that uses visible or ultraviolet (UV) light to form patterns on the photoresist through printing. Printing is understood as the process of projecting the image of the patterns onto the resist surface using a light source and a photomask. There are three types of printing −contact, proximity, and projection printing−, but only the contact mode is used in this work. When a contact aligner is used, the resist is directly placed in contact with the photomask minimizing possible diffraction effects. Thus, a cleaning of the mask should be constantly carried out to avoid possible contamination of the mask that could degrade the lithographic outcomes.

Mask aligner

The equipment used for printing is a contact mask aligner with a Hg lamp of 350 W without optical selective system. Such an apparatus is located in the facilities of Universität Süd cleanroom that is heading by Prof. Dr. Paul Ziemann from the Department of Solid State Physics.

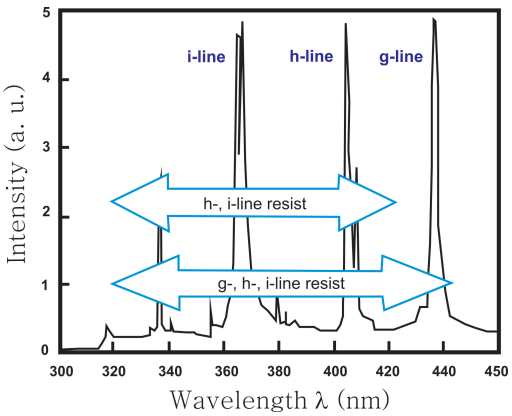


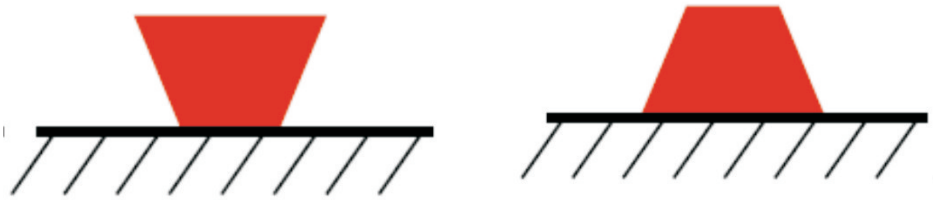
Figure 2.1: Mercury lamp spectrum. Taken from (25)

The typical emission spectrum of a mask aligner with Hg light source without an optical selective system consists of three main emission peaks at 365 nm (i-line), 405 nm (h-line) and 435 nm (g-line), as shown in Figure 2.1. The measured output intensity, by

means of a photodetector, is $10,2 \pm 0.05$ mW/cm^2. The negative resist, which is explained in next section, is sensitive to a narrower absorption spectrum, indeed, only to the i-line corresponding to 365 nm.

Photoresist

Photoresists are classified in two manners, in negative and positive tones. After exposure of a negative resist, the unexposed region in the resist are held soluble to a proper chemical solution (developer). On the contrary, the exposed parts become insoluble to the developer due to a cross-linking process between the polymers. A typical profile for a negative resist, after development, is seen in Figure 2.2a. The undercut might be varied by changing the exposure dose. A small exposure dose produces a pronounced undercut, whereas a high exposure dose does a weak undercut (25).



(a) (b)

Figure 2.2: Negative and positive resist profiles. Taken from (26)

In positive resist, the exposed parts are soluble to a resist developer as a consequence of breaking bonds in the polymer chain. In addition, unexposed parts remain insoluble unless they undergo UV light exposure. The common profile encountered for a positive tone resist in depicted in Figure 2.2b.

At the scales of patterned structures by photolithography, diffraction effects play a fundamental role. This effects the edge profile (side-wall) of the resist. As a result, characteristic side-walls are found, as shown in Figure 2.2. In the case of a positive resist, the intensity broadening is less close to interface mask-resist and increases towards interface resist-substrate (27). This gives as a result a

positively sloped sidewall. The same principle is true for a negative resist where the side-wall attained is typically called undercut.

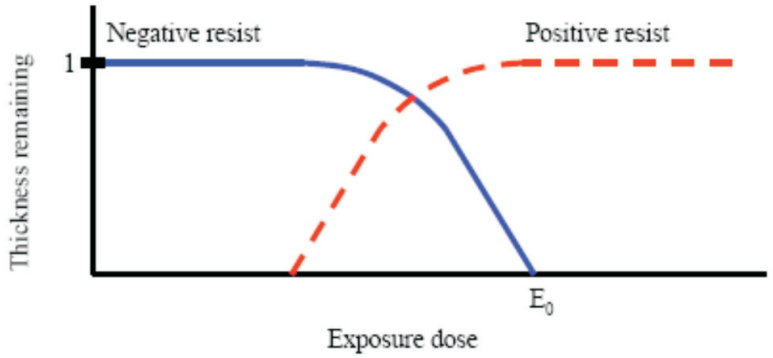


Figure 2.3: Contrast curve of a positive and negative resist plots, the remaining resist thickness as a function of the (logarithmical plotted) exposure dose. For a negative resist, E_0 corresponds the exposure to clear all resist. In the case of a positive resist, E_0 is the lowest required dose to keep resist thickness remaining Taken from (26)

The contrast of a resist defines the development rate as a function of the absorbed light dose, see Figure 2.3. A photoresist with high contrast exhibits less dark erosion, allowing straight side-walls (25). In this work a negative resist AZ® nLOF 2070 is employed to be patterned. Among the most outstanding features of this resist stand out the following

- It has very high thermal stability allowing hard-bake up to 250 °C without a rounding of the cross-linked resist patterned.
- It is very stable to alkaline environments, which makes it a suitable resist mask for the electroplating process. It is not soluble in many organic solvents[1].
- It is sensitive to be patterned by means of e-beam lithography thus allowing a combination of fast UV and high-resolution e-beam lithography.

[1] not stable against KOH

- Its negative profile allows a straightforward lift-off process
- Its high contrast permits the acquisition of smooth and straight side-walls.

Mask Fabrication

The first step in optical lithography is to create a mask. The mask substrate is commonly borosilicate glass or more recently fused-silica because of its lower thermal expansion coefficient and higher transmission at lower wavelengths (28). Our mask design consist of an array of 9 surface-electrode structures with more than 60 RF and DC electrode patterns, as shown in Figure 2.4.

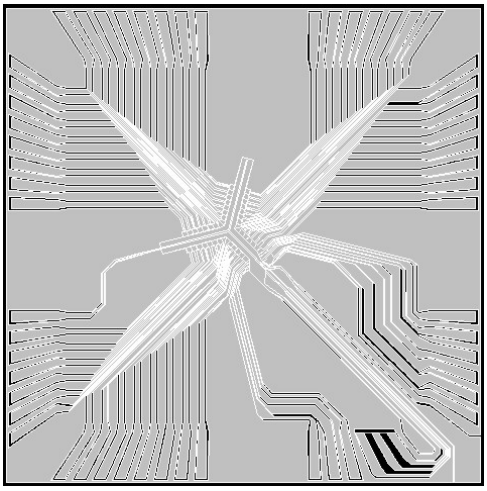


Figure 2.4: Mask Design

In our mask design there are small and large Y-junctions as well as the space between future electrodes is varied from 1.0 μm until 2.6 μm. The grey regions in Figure 2.4 represent the parts where the Cr, in the physical mask, should stand. Consequently, the black regions correspond to transparent zones where the UV light should pass and cross-link a negative resist to produce remaining developed resist lines.

The mask is purchased from ML&C GmbH (www.mlc-jena.de) mask producer company and essentially pursues the following procedure. As a first step, a Cr/CrO_2 layer is formed by sputtering, onto a quartz substrate, followed by

photoresist (PR) coating on top of it, as seen in Figure 2.5a. A certain lithographic pattern, by using e-beam or laser lithography equipment, is written on the surface of the PR layer, see Figure 2.5b. The pattern formed on the PR, by using an appropriate developer, is finalized over the PR area which was exposed by the lithography equipment, as displayed in Figure 2.5c. By employing either a dry or wet etching technique, the exposed Cr/CrO_2 area is etched to reveal the quartz surface, as bared in Figure 2.5d. In this last step, the area covered by the photoresist is unaffected. The remaining photoresist is removed via a strip process, followed by clean and dry steps. At this stage, the photomask surface consists of dark and clear areas (dark areas are still covered by Cr/CrO2 whereas clear areas are naked quartz, which transmits the incoming light source, as shown in Figure 2.5e. A critical dimension (CD) measurement is carried out over the dark or clear space patterns, as depicted in Figure 2.5f. Positional accuracy of the original patterns is measured, as illustrated in Figure 2.5g. The next step consists on identifying defects and, if needed, necessary repair work is performed in order to ensure corroboration to the design, see Figure 2.5h. Possible particles are removed by utilizing a cleaning step, as portrayed in 2.5i. Finally, a pellicle is mounted over the finished side of the quartz wafer in order to avoid a potential contamination, as represented in Figure 2.5j.

(a) Sputtering of Cr/CrO_2

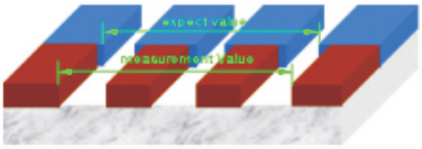
(b) Patterning by e-beam or laser lithography

(c) Development of photoresist

(d) Dry or wet etching

(e) Stripping process

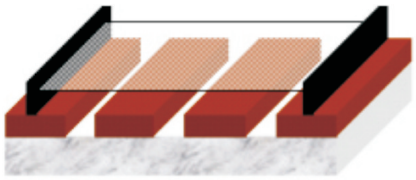
(f) CD measurement



(g) Positional accuracy measurements

(h) Identification of defects

(i) Cleaning step



(j) Pellicle mounting

Figure 2.5: Mask fabrication procedure. Taken from (29)

2.2 Deposition

If a thin film of certain material is deposited onto a substrate or onto a previously deposited layer, we do refer to the term deposition. The range of deposition thickness varies in accordance to the deposition method employed. The deposition can be made in a control way allowing to grow material from single atomic layer by using molecular beam epitaxy (MBE) until some micrometers by means of electroplating[1]. Deposition is useful in a wide range of applications and depending on the requirements a specific method is utilized. Deposition methods can roughly be categorized in two classes, regarding whether the principle is physical or chemical. Although there are methods which fall outside these two categories, relying on a mixture between physical and chemical means such as MBE and reactive sputtering. In this work two deposition methods are used, each physical and chemical, and are the scope of the following sections.

2.2.1 Thermal Evaporation

The thermal evaporation deposition uses physical means to pile up material onto another. This physical deposition technique consists in heating until evaporation of the raw material to be deposited. The material vapor is addressed in a conic beam, as shown in Figure 2.6, and finally condenses in form of a thin film on the cold substrate surface as well as on the vacuum chamber walls (26).

To avoid any reaction between the vapor and the atmosphere usually low pressures about 10^{-6} or 10^{-7} mbar are used. In addition, at these low pressures, the mean free path (mfp) of vapor atoms is in the order of the vacuum chamber dimensions, which allows that the vapor particles travel straightforward from the evaporation source until they deposit onto the substrate. By doing so, a phenomena called *shadowing* avoids that the side-walls of a 3D object to be deposited.

Among thermal evaporation techniques, there exist different methods that can be applied to heat the material to be deposited. In our case, the deposition setup in the Universität Süd cleanroom facilities uses resistance heating (Joule

[1] it also is found as *plating*.

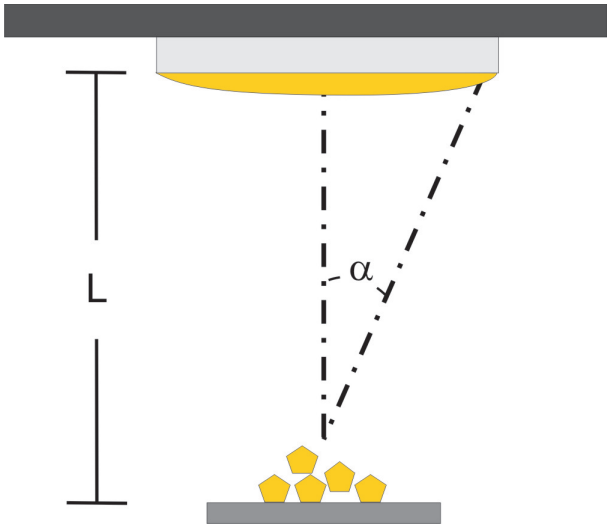


Figure 2.6: Thermal evaporation.

effect) and bombardment with a high energy electron beam (electron beam heating). During the thermal deposition onto the glass substrates[1], the material is evaporated by using the resistance heating. The material is heated until fusion by means of an electrical current passing through a metal plate where the raw material is located (Joule effect). The evaporated material is straightforwardly directed and condensed on the substrate. Thermal deposition has some important advantages such as it is simple and results convenient for depositing Cr and Au that have low fusion temperature.

As it is seen in Figure 2.6, there is a limited region in the substrate holder where the thickness of the deposited material is uniformly grown. This limits the number of glass substrate to be coated by the evaporated material. In this work, I located inside the thermal deposition chamber within four and six 1" diameter glass wafers in order to accomplish more reproducible results. The thickness deposition is measured with a quartz piezoelectric monitor where is located within the range of homogenous thickness. As a first step, I carried out the deposition of a Cr layer to enhance the adhesion between Au and the glass substrate. As as successive step I deposited a Au layer as a seed layer for electroplating. Specific

[1]see section 4.2

thicknesses and deposition rates employed are given in Chapter 4.

2.2.2 Electroplating

In general, to electroplate a certain substrate one has to place the substrate in a solution containing a metal salt and connect it to a current supply as a cathode. Prior to that, a seed layer of a conductive material must be deposited onto our particular substrate in order to enrich film uniformity and adhesion. On the other hand, the anode is a plate of a distinct conducting material. During electroplating positive ions of the metal are attracted to the cathode substrate and grow up a film when a current between cathode and anode is applied (26).

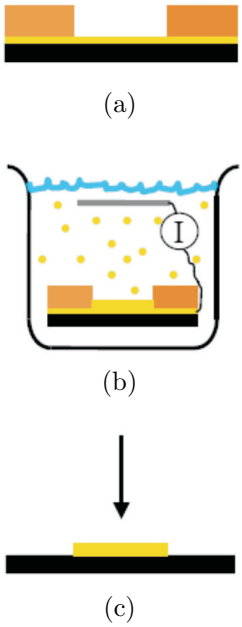


Figure 2.7: Electroplating process. Modified from (26)

In this work, the gold plating is carried out in the following manner. The glass substrates are coated by a Au/Cr bilayer which enriches the adhesion to glass surface, due to the Cr layer, and good electrical contact, due to the Au seed layer. This bilayer coating is performed by thermal deposition means as described in the previous section. A negative resist is spun onto the Au/Cr bilayer and patterned via photolitography, as shown in Figure 2.7a. After development, a *resist mask* is

obtained, which has the function to stand the electroplating process whereas the Au layer is grown in the places where the resist does not cover the Au seed layer, as seen in Figure 2.7b. This selective growth makes the electroplating process a simpler and more economical process compared to evaporation and sputtering. The aspect ratios achieved during electroplating process are only limited by the aspect ratio of the resist itself. This brings out another dazzling advantage when high aspect ratios of plated structured are required. Although in the electroplated metal films the thicker the plated layer is the larger the surface roughness and grain size are (26). It is suggested that via mechanical chemical polishing (MCP) process this plated roughness might be reduced [1](25) . Once the desired thickness and zones are plated, the resist mask is either stripped and/or removed from the plated structure. The final step is to etch away the Au seed layer, as depicted in Figure 2.7c. The etching mechanism is the scope of the next section.

2.3 Etching

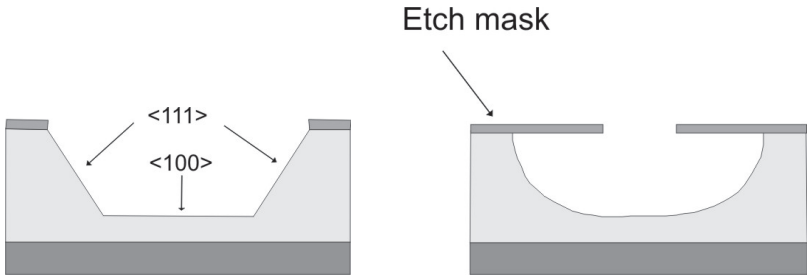
Usually the etching process is subdivided in two main classes. Firstly, *wet etching* where the material to be etched in is dissolved when soaked in an appropriate chemical solution. Secondly, *dry etching* where a vapor etchant or sputtering is used to dissolve the material. In the following, we shall explain this two processes.

2.3.1 Wet Etching

Within etching process this is the simplest method. It only demands to immerse the material in an appropriate etching solution (etchant). There might be some drawbacks as the fact that in order to selectively etch the material of interest, the mask should stand against the etchant, or at least it should have lower etch rate. Typically, due to its nature the wet etching process yields in the material of interest, isotropic etching, which is a homogenous etching in all directions. As a consequence, the etching profiles due to the latter are rounded side-walls, as seen in Figure 2.8a. Anisotropic etching in contrast to isotropic etching means the

[1] A future work would be the possibility to implement MCP after electroplating so as to achieve a lower surface roughness

material is etched with different etch rates in different directions. To illustrate anisotropic wet etching, we take the elegant example when etching a silicon wafer in a chemical such as potassium hydroxide (KOH). The straight side-walls correspond to the $< 111 >$ crystal plane when etching a hole in a $< 100 >$ direction. As a result, a pyramid-like profile instead of a hole with rounded side-walls is observed, as depicted in Figure 2.8b. The principle of anisotropic and isotropic wet etching is schematically shown in the Figure 2.8. Wet etching is used in this



(a) Anisotropic (b) Isotropic

Figure 2.8: Wet etching process.

thesis to etch the Au seed layer and the Cr adhesion layer, to assure good electrical contact. After etching of the seed layer a visible increment in the surface roughness is observed. However, it is known that the surface roughness of the etched material can be improved somewhat by optimizing the etchant concentration and temperature, and by using ultrasonic to ensure a constant supply of fresh etchant to the interface (30).

2.3.2 Dry Etching

Although, the dry etching process can be divided in three different classes, so to speak, reactive ion etching (RIE), sputter etching, and vapor phase etching, in this thesis, only RIE is of interest.

Typically, the material to be etched is situated inside a cylindrical reactor in which different gases may be introduced, as seen in Figure 2.9. A RIE reactor works by applying a strong radio frequency (RF) electromagnetic field to the

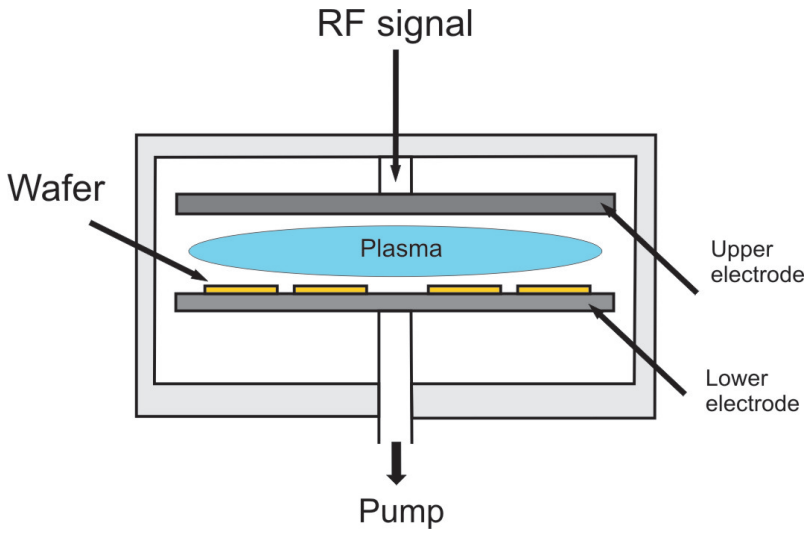


Figure 2.9: Scheme of a $RIEO_2$ reactor

wafer holder (lower electrode in Figure 2.9). The RF oscillating field creates a ion plasma by removing electrons from the gas molecules. In RIE, there exist both physical and chemical means when removing the material from a substrate.

In the chemical part of RIE, the generated ions are accelerated towards the wafer holder and react at the surface of the material being etched, forming another gaseous material.

On the other hand, the physical part in essence is similar to sputtering deposition process. When the ions have high enough energy, they transfer their kinetic energy to the material to be etched, thus sputtering or knocking off atoms out of the material. As a result of a near vertical deliver of the reactive ions anisotropic etching profiles are feasible. A schematic picture of a reactive ion etching system is shown in the Figure 2.9.

In this work, reactive ion etching in oxygen environment ($RIEO_2$) is utilized as complementary stripping process to fully remove the resist residues after a partial stripping of the resist mask in NMP[1].

[1]See section 4.5

Chapter 3

Chip Fabrication Outline

Great things are done by a series of small things brought together.

Vincent van Gogh

Processing techniques, which some of them are made clear in Chapter 2, bring us many feasible paths or layouts in which the required chip can be constructed. In addition, correct compatibility between processing steps and materials should be sought in order to achieve thriving results. As a particular example, a chose resist must completely stand an electroplating bath based on suitability between resist and bath chemical properties. Therefore, an appropriate resist choice for electroplating may prevent obstacles towards further fabrication steps and finally fruitful intended device. Another possibility we can pursue for successful fabrication might be matches between substrate, starting layer and resist etching features. In this chapter, various comparisons between possible and chose intermediate steps for fabrication outline are presented. As far as possible, examples of reported works are depicted intending to support the selection of respective fabrication steps.

3.1 Fabrication scheme

Earlier attempts show that, due to its simple geometry, a surface-electrode ion trap might be manufactured by conventional photolitography and deposition as main processes (18). Many questions might emerge as consequence of choosing

certain route toward final device achievement. Nevertheless, to swerve previous mentioned obstacles, we can select each of those small steps based on a fundamental criterion. Intermediate fabrication steps should be as simple as possible, compatible each other, and bring all together a not complex fabrication layout. We can envision a prolific fabrication scheme when fulfillment of this requirement is realized by carefully selecting matches within well-known and uncomplicated processes. Fabrication layout is illustrated in Figure 3.1, which brings us many advantages upon other possible plans.

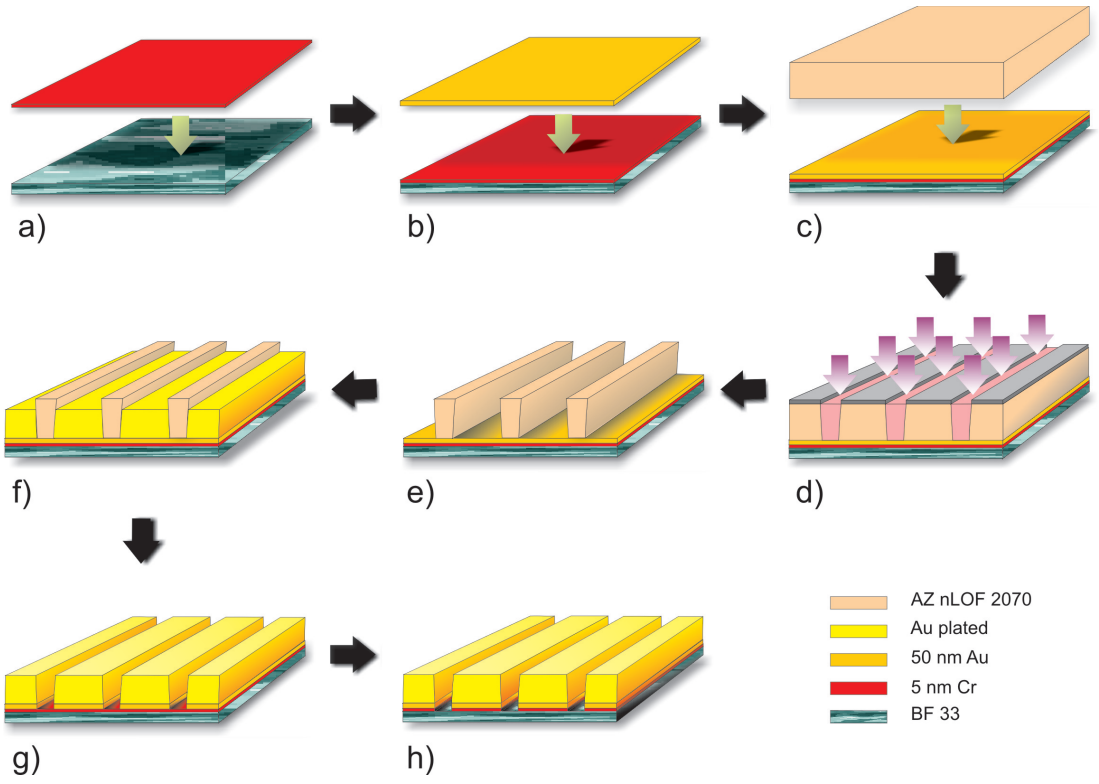


Figure 3.1: A scheme of fabrication process. a) Evaporation of the adhesion Cr layer on BF® 33 wafer, b) Evaporation of the starting Au layer on Cr/BF® 33, c) Spin coating of AZ nLOF 2070 resist, d) Exposure to UV light, e) Development, f) Electroplating of Au, g) Stripping of resist, h) Wet-etching of Cr and Au layers.

Firstly, for a selected substrate, significant stiffness and hardness, additionally to surface-electrode ion trap operation features[1] are mandatory. It is known that, additional to high loss tangent and low dielectric strength, Si wafers do not offer high stiffness and hardness. Despite, insulating properties can be tuned by doping, mechanical properties cannot. In order to accomplish mechanical stability and fully satisfy ion trap operation requirements, among most suitable substrates stand out saphire, quartz (14) and BOROFLOAT® 33. Since surface-electrode ion trap demands a substrate with very high dielectric strength and low loss tangent, saphire and quartz seem to be the most appropriate candidates. In spite of this, the rms roughness of shapire is quite high compared to the one from BF® 33 and quartz, which reduces ion trap operation due to an increment of heating rate as a function of ion trap surface roughness (31). Although physical features of quartz surpasses BF® 33, the latest one has the advantage to be more commercial, easier and cheaper in manufacturing (28).

To ensure proper sticking of conductive material to substrate, an adhesion promoter should be used as intermediate layer. This adhesion layer must stick to both substrate and subsequent conductive layer. Conventionally, Cr, Ti and Ti/Pd are eligible to enhance adhesion properties between non-compatible materials. Furthermore, this layer should be easy to remove or etch in the final fabrication step to assure exceptional insulating characteristics for ion trap. Despite Cr adhesion layer presents a diffusion process, when it is heated up to 350 °C, it also exhibits more advantages compared to Ti or Ti/Pd layers. From one side, Cr etchant does not dissolve or attack borosilicate glass type whereas typical Ti etchants significatively etch borosilicate substrates (25). As consequence, Cr etching results in a clean and selective process, where etch rates can be controlled, as I shall show, by diluting Cr etchant in water. Although Ti and Ti/Pd can be effectively etched they bring about more complicated processes as the use, as removal process, of RIE or even dangerous like HF, as etchant, sacrificing part of borosilicate substrates. Thus, as it is portrayed in Figure 3.1a a Cr layer is placed on a properly[2] cleaned BF® 33 wafer by thermal deposition means.

[1] See section 1.3 and 4.1

[2] See section 4.1.1

Posterior deposition of adhesion layer a well-conductive material should be piled up to promote better electroplating conditions by increasing conductivity during the electrochemical growth. Conventionally, either Ni, Cu or Au are utilized as starting layer for electroplating. Since a material with non-oxidizing properties is of interest for ion trap performance, Au is deposited on top of Cr/BF®33 by thermal evaporation, as it is displayed in Figure 3.1b. Additional benefits that thin Au layer offers is its capability to be etched by wet etching[1], or even, a bit challenging by dry etching (32; 33).

After deposition of Au starting layer potential photoresist should be coated on Au/Cr/BF33. Amongst several types of photoresist stand out AZ nLOF 2070 and AZ9320, which are high aspect ratio and high contrast resists, as well as they stand electroplating process when no alkaline solution with a pH $>$ 10 is devoted. Main difference between AZ nLOF 2070 and AZ9320 is located as, they are negative and positive resists, respectively. Although, AZ9320 resist can reach aspect ratios larger than 20, AZ nLOF 2070 is of more interest since its high aspect ratio up to 4, allows us to succeed the intended aspect ratio for shielding factor[2]. Moreover, its negative profile permits a thermal evaporation of a superconductive material, which might improve operation of microtrap. As it is shown in Figure 3.1c, elected resist is placed on coated substrate by using spin coating.

Optical lithography has the benefit to request lees and easier steps compared to other sophisticated processes such as LIGA, deep ultra-violet (DUV), and electron beam lithography. What is more, due to the fact that the whole structure of microtrap lie on a plane, there is no need of initial or consecutive alignment. Therefore, resist exposure is executed as illustrated in Figure 3.1d. During development, Figure 3.1e, the dark parts are dissolved and anticipated structures are acquired.

Electroplating reveals many advantages upon other possible processes. By using sputtering process mask resist can be damage and some Au can redeposit on sidewall resist, which might make resist removal rather than complicated. On the other hand, evaporation should be carefully carried out in order to attain large

[1] See section 4.6

[2] See section 1.3

mean free path (mfp) of evaporated material to guarantee no deposition on sidewalls (shadowing effect). Only when a large mfp is fully achieved, no deposition of Au can be present on resist sidewalls and stripping or lift-off process would be simple. Compared to sputtering and evaporation, electroplating allows trouble-free removal of mask resist. As we shall show in section 4.4, when electroplating parameters are carefully manipulated, growth of Au on mask resist is diminished thus making stripping of resist feasible. Considering previous pros and cons, as it yields a noticeable surface roughness, we have opted to grow Au electrodes by electrochemical means, as it is pictured in Figure 3.1f.

Stripping of AZ nLOF 2070 is schematically described in Figure 3.1g, where resist is removing either by wet or dry cleaning. As ultimate steps, Au and Cr layers are etched by using corresponding etchants[1]. It ensures, by controlling etching parameters, best insulation between electrodes as it is represented in Figure 3.1h.

Up to here, main intermediate steps have been discussed in order to briefly show our prefer path to achieve our looked-for ion trap chip. In the next chapter, results due to experimental process, trials of every steps, as well as most fruitful results are explicated in detail.

[1] See section 4.24

Chapter 4

Ion Trap Chip Fabrication

Mache die Dinge so einfach wie möglich - aber nicht einfacher.

Albert Einstein

The fabrication process is hierarchical in nature in the sense that it inherits a cascade behavior in which a previous flourishing step itself precedes a further booming step. This chapter encompasses detailed experimental results about the whole fabrication procedure. In particular, examples of encountered errors and trials are intended to give a wider overview of the manufacturing process.

On the other hand, as it has been previously discussed, one looks for an optimal substrate with exceptional electrical properties. Next section is addressed to underline the significance of using borosilicate glass as a reliable substrate. Many advantages, specially, insulating as well as thermal draw highly our attention to finally work with this type of glass.

4.1 Borosilicate Glass

In a previous chapter I have underlined the advantages of using a borosilicate glass compared to quartz and shappire. In summary, I decided to work with a borosilicate glass beacuase, compared to quartz, is much cheaper and easier. On the other hand, it has a lower surface roughness when compared to saphire.

Specifically, BOROFLOAT® 33 (BF®33), is a borosilicate glass type 3.3[1] and it was purchased from Plan Optik A. G. (www.planoptik.com). It is a high quality glass with outstanding physical and chemical properties. It is highly resistant to attack by water, strong acids, alkalis and organic substances. Moreover, as shown in Table 4.1, its low thermal expansion, high thermal shock resistance, ability to withstand temperatures above 450 °C, low loss tangent and high dielectric strength make it a suitable substrate for surface-electrode ion trap operation.

Table 4.1: Main physical properties of BOROFLOAT® 33 for chip fabrication

Property		Value
Coefficient of Linear Thermal Expansion (CTE)	$\alpha_{(20-300°C)}$	3.25×10^{-6} K^{-1}
Loss Tangent ($tan\,\delta$)	25 °C, 1 MHz	37×10^{-4}
Dielectric Strength		> 9000 kV/cm
High Operation Temperature	< 10 h	500 °C

In addition, BF® 33 has an excellent mirror-like surface, a high degree of flatness and an excellent optical quality. Its chemical composition makes it a unique material, where thanks to its low alkali content, around 4 % in Figure 4.1, compared to nearly all other glasses, makes it an outstanding electrical insulator (28).

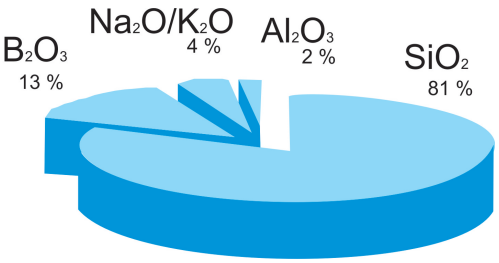


Figure 4.1: Chemical Composition of BOROFLOAT® 33. Taken from (28)

Specific information about purchased BF®33 wafers is displayed in Table 4.2. Although, larger diameters such as 2" or 3" are possible for fabrication, they do not bring out more advantages. Due to the larger dimensions a cleaving process prior to photolithography patterning might release some dirt particles on the wafers. It would not be easy to handle it since laboratory equipment such as larger beakers and more amount of

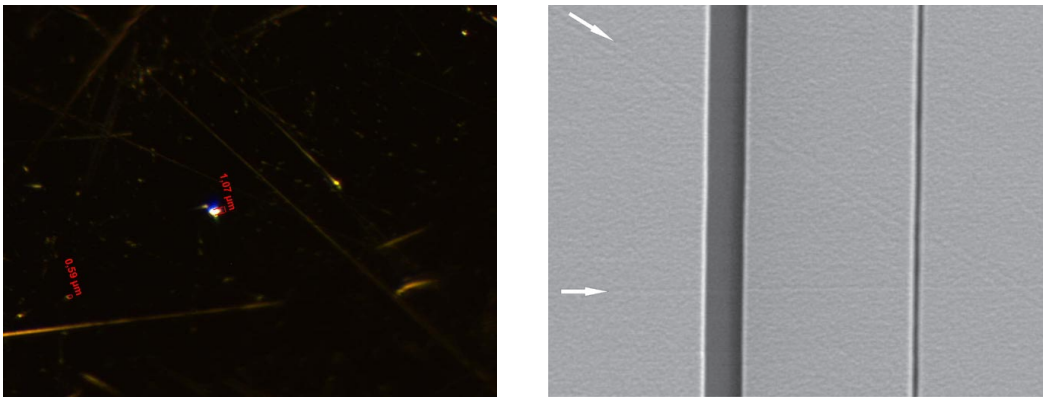
[1] As specified in the international standard ISO 3585 and EN 1748 T1

solvent are necessary. The wafers employed in this thesis have 1" diameter and thickness of 0.7 ± 0.07 mm. Moreover, thinner wafers are expected to bring us better results in the cleaving process.

Table 4.2: Specifications from BOROFLOAT® 33 wafers

Parameter	Value
Diameter	$\emptyset\, 25.4 \pm 0.3\,\mathrm{mm}$
Thickness	$0.500 \pm 0.025\,\mathrm{mm}$
Polishing	$R_a < 1.5\,\mathrm{nm}$

The mean roughness, is an important and fundamental factor since it transfers to successive starting Cr/Au layer and later on electroplated gold surface, as rendered in Figure 4.2.



(a) Dark-field optical micrograph of Au/Cr bilayer (x50)

(b) SEM image of electroplated Au layer of 1.74 μm

Figure 4.2: The presence of scratches as a result of the polishing process influence the deposited layer roughness in further fabrication steps such as a) Au seed layer and/or b) Au plated electrodes.

The Atomic Force Microscopy (AFM) measurements were carried out in the Institute of Optoelectronics facilities in the west part of University of Ulm, under the supervision of Kamran Forghani. AFM studies prior to, and after, cleaning are done to determine the wafers roughness. As we can see from Figure 4.3a,

when no cleaning process is performed, glass wafers present a mean roughness of $R_a = 0.836$ nm as well as some defects and holes due to the polishing process. On the other hand, and particularly, when acetone and isopropanol are devoted as cleaners[1], some solvent residues remain on glass surface, as appeared in Figure 4.3b. Importance of a profitable cleaning process is discussed in next section. As I shall portray, strong influence of remained dirt on wafer avoid any further step.

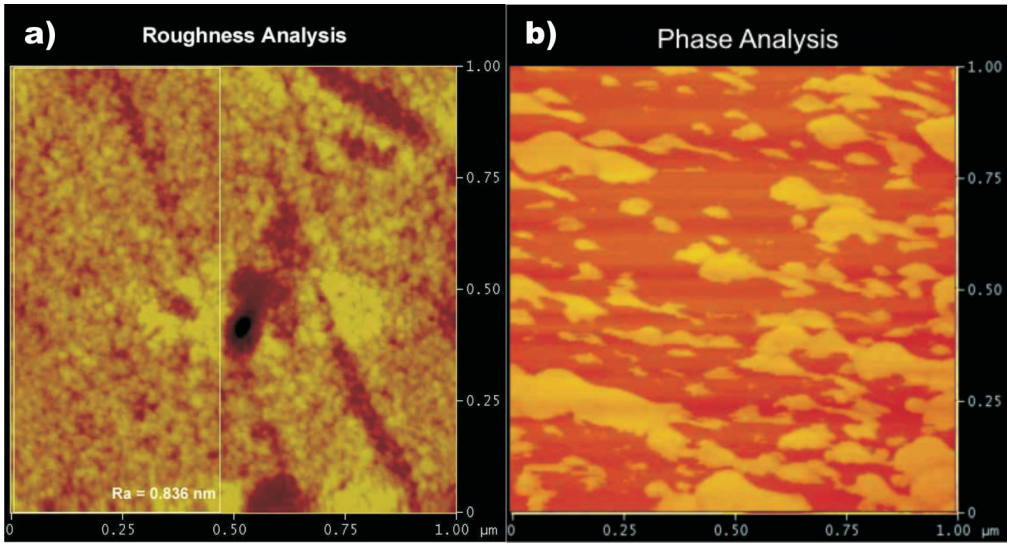


Figure 4.3: AFM topography illustrating a: a) non-cleaned and b) after two-stage process cleaned BOROFLOAT® 33 wafer of $1 \times 1\,\mu m^2$.

4.1.1 Wafer Cleaning

Conventional substrate cleaning process might vary regarding the sort of dirt that is present on substrate. When organic residues lie on the substrates a solution so-called piranha[2] is preferentially used. On the other hand, if metallic dirt on the wafer surface is present a so-called RCA[3] solution might be employed.

BOROFLOAT® 33 Glass wafers exhibit originally dirt particles up to $28\,\mu m$, as measured in Figure 4.4. After efforts by employing both piranha and RCA

[1] For more details about intended cleaning process see Section 4.1.1
[2] A mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2)
[3] A mixture of hydrochloridic acid (HCl) and hydrogen peroxide (H_2O_2)

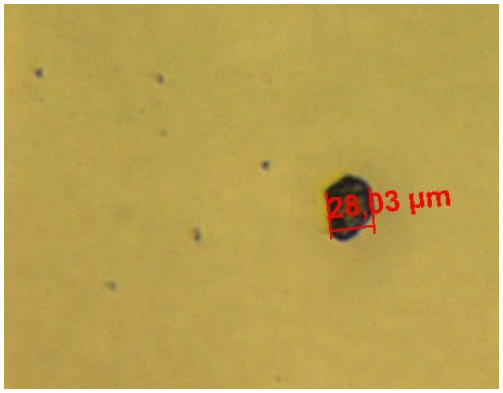


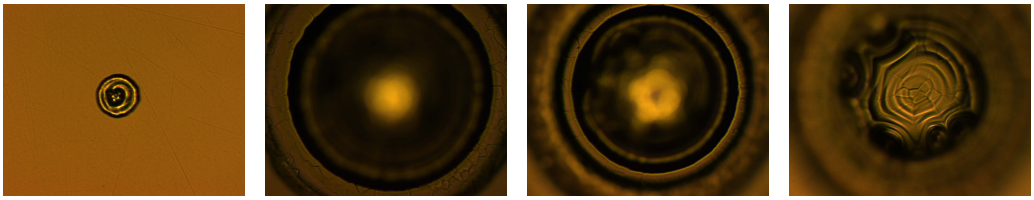
Figure 4.4: Optical micrograph showing dirt on BOROFLOAT® 33 before cleaning process (x100)

solution, there are still particles left on the substrate, such that, those particles do not seem either glassy or metallic. Since no success regarding conventional cleaning processes (two-stage, piranha and RCA) of borosilicate glass was found, an alternative method is developed where mechanical and chemical means are combined to get rid of dust and other non-desirable dirt on the glass wafers.

Two-stage process

Traditionally, if Si wafers are contaminated with particles and/or organic impurities a cleaning process so-called two-stage is used. This process is performed as follows. Wafers pieces, previously cut or cleaved by using a diamond tip, are soaked in a small amount of acetone (CH_3COCH_3), for 3 minutes in an ultrasonic bath (100 %), which removes organic impurities. A successive wash in a small amount of isopropanol (C_3H_8O), for 3 minutes in an ultrasonic bath (100 %), eliminates the contaminated acetone. Afterward, wafer pieces are heated up for 2 minutes at 120 °C on a hotplate, to evaporate possible solvent residues. Posterior cleaning, resist coating should be immediately done to avoid possible water adsorption (25).

Although the two-stage process is employed to properly clean Si wafers, BF®33 wafers demand a different cleaning process. If one tries either individual or multiple conventional processes no appreciable attainment is perceived. As explained in Figure 4.5 the gold grains affect, on the substrate, areas larger than 10000 μm^2 when a two-stage method is carried out on the glass substrates. This kind of grain is got after deposition of Au/Cr on a glass wafer previously cleaned by



(a) Grain $> 1000\,\mu m^2$ (b) Bottom (c) Middle (d) Top

Figure 4.5: A sample which was previously cleaned by means of the two-stage process presented gold grains with an area up to $10000\,\mu m$ after the deposition of 5 nm Cr layer and a successive 50 nm Au layer. A series of defocus technique permits to observe the bottom, middle and top part of the grain. This results strongly suggested to seek for an alternative cleaning method since such large grains visibly prevent any successful lithographic outcomes

employing two-stage method. Without a doubt, these type of dirt clearly inhibits any sequential step. Hence, to get best results for glass wafers a combined method by using spin coater, commercial cleaner and a lab tip is developed. This method is specified as follows.

Spin Coater as cleaner

To attain positive results during whole fabrication process a fruitful cleaning process is required. Since possible dirt particles may affect the developed resist lines and as consequence create probable shortcuts between electrodes, those particles should be strongly prevented.

For proper cleaning of BF® 33 wafer, considerable amount of AJAX®, a commercial glass cleaner, is applied on glass surface. Whereas operating spin coating machine at 2000 rpm for 40 s, with an initial slope of 400 rpm/s, a sponge lab tip slightly sweeps glass surface and moves rotating itself from glass center towards wafer edge. This step should be done as slow as possible intending to homogenously remove most of the dirt on glass surface.

After sweeping of the glass surface with AJAX® and a lab tip, plenty of water on the wafer is spilled, while two successive spinning processes should be executed. The first one is done at 2000 rpm for 40 s, and it removes cleaner residues as well

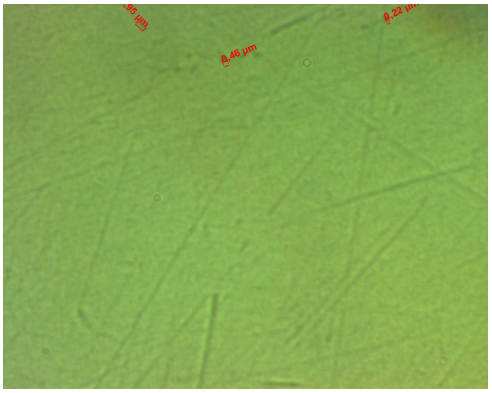


Figure 4.6: Thriving results achieved by employing the spin coater method. There is no considerable dirt on glass surface after this process. Although, some dirt particles below 1 μm are observed, which might not strongly affect the resist patterned structures. (x100)

as big particles. Whereas a second one at 7000 rpm for 40 s, is to guarantee better removal of small remaining dirt particles, due to high centrifugal force and collisions water-dirt particles that might overcome adhesion force between dirt particles and glass surface. After rinsing the sample with water, it is dried by using a N_2 gun, followed by placing it on a hotplate for 5 min to evaporate water residues. Posterior this cleaning process best results are obtained as one can see in Figure 4.6.

Notwithstanding there still exist some dirt particles, their size is reduced below 1 μm. This dirt average size is pleasingly acceptable, under our purpose, where negative resist lines larger than 1 μm are intended. Once a prolific cleaning process is scoped a succeeding thermal evaporation of an adhesion layer as well as a gold seed (starting) layer can be performed as they are altogether explained in next section.

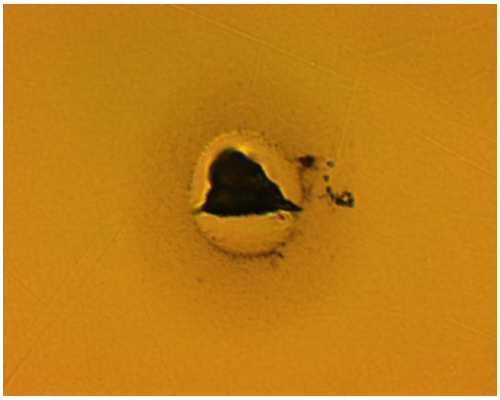
4.2 Thermal Evaporation

Well cleaned wafers, by using the spin coater method, are placed in a vacuum chamber at 2.3 x 10^{-7} mbar where high vacuum condition is reached by using a turbomolecular pump. Once this pressure is grasped, thermal evaporation deposition may start.

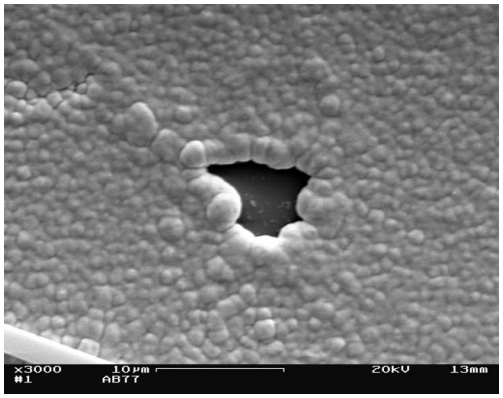
Initial thermal evaporation processes are intended by depositing a 2.3 nm[1] Cr layer and a 30.0 nm Au layer. However, this Cr layer is not enough to com-

[1]Thickness based on the piezoelectric crystal monitor

pletely adhere the succeeding Au layer since visible holes appeared under optical microscope studies, as shown in Figure 4.7a. A more evident influence of holes is discerned after electroplating process, as shown SEM pictures in Figure 4.7b. Consequently, a second bilayer Au/Cr is chosen which shows an improved sticking quality as well as an acceptable Au surface roughness to start the electroplating growth.



(a) Optical micrograph showing a hole in a starting Au/Cr bilayer of 30.0/2.3 nm



(b) SEM image showing the influence of a hole in a bilayer Au/Cr through an electroplated Au layer of 1.74 μm

Figure 4.7: The original Cr deposited layer of 2.3 nm presented poor adhesion between gold and glass it is seen by the presence of holes after thermal deposition and electroplating

Previous surface topography studies of the thermal deposited gold layer indicate that its percent ratio of rms[1] roughness decreases as its nominal film thickness layer increases from 10-150 nm (34). The thermal deposition of a too thin Au seed layer might not be ensure good electrical contact and electroplating performance could be reduced. On the other hand, a deposition of thick Au seed layer cause an increment in the surface roughnes of the seed layer which is transmitted to plated Au layer. A good balance between roughness and minor thickness for Au wet-etching is a 50 nm layer. Therefore, final evaporation parameters are

[1]root mean square

chosen as follows: i) a 5.0 nm Cr layer with a deposition rate of 0.2 Å/s and ii) a succeeding 50.0 nm Au starting layer with deposition rate of 1.2 Å/s.

4.3 Optical Lithography

So that to achieve fruitful results for the intended ion trap chip an optimum photolithography process should be attained. As I shall indicate in this section, prime lithographic parameters depend not only on exposure dose but also on resist thickness, soft-bake, post-exposure bake and development. Since many parameters are involved a better description of what has been done is written in section 4.3.6. Prior to this lithographic output, individual achievements of resist coating, soft-bake, exposure dose, post-exposure bake and development time are discussed. By doing so, I intend to give first the background, of every parameter in order to finally understand the results in terms of a whole system which is a function of many variables. A multi-variable dependant function must be treated in such a way that each variable can be optimized as far as the rest are kept constant. Mathematically, a well-behaved optimization function $O_f(x_1, x_2, ..., x_n) = L(x_1, x_2, ..., x_n)$ has a minimum or optimized point if: i) $\frac{\delta L}{\delta x_1} + \frac{\delta L}{\delta x_2} + ... + \frac{\delta L}{\delta x_n} = 0$; ii) for a minimum $\frac{\delta^2 L}{\delta x_i \delta x_i}, \frac{\delta^2 L}{\delta x_j \delta x_j}, ..., \frac{\delta^2 L}{\delta x_n \delta x_n} > 0$ or for a maximum $\frac{\delta^2 L}{\delta x_i \delta x_i}, \frac{\delta^2 L}{\delta x_j \delta x_j}, ..., \frac{\delta^2 L}{\delta x_n \delta x_n} < 0$; and iii) $\frac{\delta^2 L}{\delta x_i \delta x_i} \times \frac{\delta^2 L}{\delta x_j \delta x_j} > (\frac{\delta^2 L}{\delta x_i \delta x_j})^2$

To experimentally approach to this optimized point, one has to adjust and find best value of the variable of interest while holding constant the rest of variables. The first parameter that can be fixed is the resist thickness by means of spin coating method, as it is illustrated in the next section.

4.3.1 Resist Coating

Spin coating process is carried out by making use of AZ® nLOF 2070 negative photoresist. During this process, by varying different spin speeds, as well as different dilution proportions, the desirable thicknesses may be attainable. In general, spin coating takes advantages from centrifugal force and viscosity of resist to obtain the required thickness.

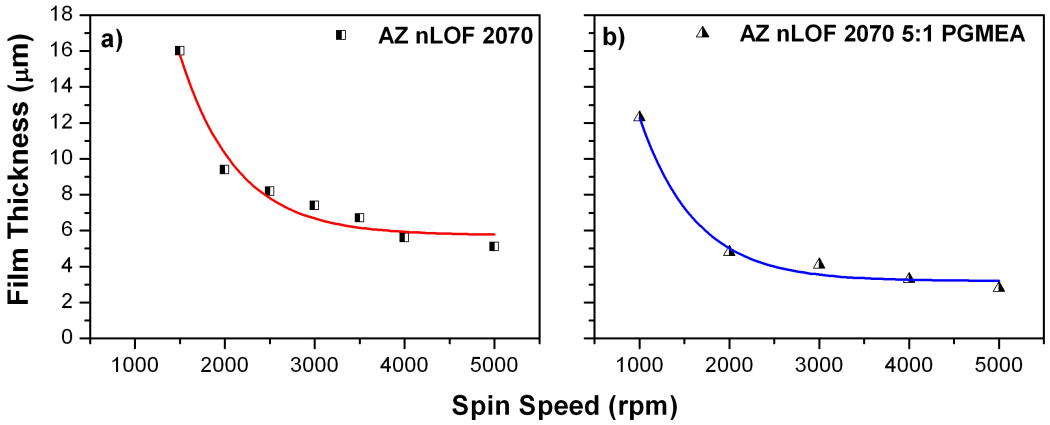


Figure 4.8: To make the spin coating process more reproducible I decided to coat Si wafer and measure the film thickness as a function of spin speed of a) non-diluted and b) diluted AZ® nLOF 2070 5:1 PGMEA resist

Although resist datasheet provides suggestive information regarding resist thickness as a function of spin speed I found small variations when solvent concentration on resist are modified. These changes could be caused due to a non-proper dilution proportions and/or resist aging. To wholly pledge finest results in photolithography I optimized thickness values by utilizing a non-diluted and diluted 5:1[1]AZ® nLOF 2070 negative resist to acquire different thicknesses as disclosed in Figure 4.8. Concerning to spin speeds, I chose different values within 1000-5000 rpm[2], which give me a wide thickness range within 2.8-16 μm. All these values are done well via taking Si wafer as substrate and with the help of an optical microscope to determine resist thickness.

To coat glass wafers the same method is implemented since no critical variation of film thickness is observed. Common resist thicknesses employed are displayed in Table 4.6, where typically values are 3.3, 3.9, 6.0 and 9.2 μm. After spin coating a pre-bake so called soft-bake is required and it is explained as follows.

[1]Dilutions ratios are based on mass proportions by means of PGMEA. From now when I refer to 5:1 AZ® nLOF 2070 I mean five times AZ® nLOF 2070 resist compared to PGMEA

[2]As a rule of thumb, spin time was fixed to be 40 s, as suggested by Microchemicals Inc.

4.3.2 Soft-Bake

Overall, it is well known that a compulsory soft-bake, prior to exposure, should be done in order to: i) avoid sticking of resist to photomask, ii) preclude popping of foaming of the resist by N_2 created during exposure[1], iii) enhance resist adhesion to the substrate and iv) reduce high **dark erosion**[2] during development (25).

Due to the solvent diffusion D_s and evaporation[3], the remaining amount of solvent in the resist is diminished when soft-baking. Solvent diffusion, which is thermally activated with the activation energy E_a, is a function of temperature T and solvent concentration C. Similarly, evaporation rate ϕ, is a function of the temperature T and the resist solvent concentration D_0, as we see in Equation (4.1).

$$D_s(C,T) = A \cdot \exp\left[-\frac{E_a}{k\,T}\right] \cdot \exp\left[-\frac{C}{\alpha + \beta\,C}\right], \;\; \phi \propto D_0 \cdot \exp\left[-\frac{{E_a}^*}{k\,T}\right] \tag{4.1}$$

Giving an insufficient soft-bake to resist a visible high dark erosion reveals making the structures less sharp and smaller than desired. Figure 4.9 shows a mousebit as a result of a poor softbaking. I found by trial and error most suitable values are within 90-110 °C, where baking time depends on film thickness. These temperatures ar also suggested by Microchemicals Inc. and allow enough amount of solvent in resist to avoid it embrittles and crackles during electroplating. Moreover, a long softbaking should be avoided, since due to decomposition of photoactive compound resist endures longer development rate (25). When a oven is needed, longer times compared to a hotplate might be involved due to a different heating process (convection). In this work, all baking processes (drying, soft-bake, post-exposure bake) are done by placing the samples in direct contact with a hotplate.

During spin coating the interface between rotating wafer and nearly static air produce on the edges of wafer turbulence, which induces a different thickness, often larger, than resist film thickness in the center of wafer. Those edge thickness

[1] This problem is not present in AZ nLOF 2070 negative resist

[2] When it happens, in our case, where negative resist is employed, exposed areas have higher dark erosion rate than non-exposed. As a result, mouse bits, holes or thinning in the exposed areas of the resist could appear

[3] rate ϕ thermally activated with the activation energy ${E_a}^*$

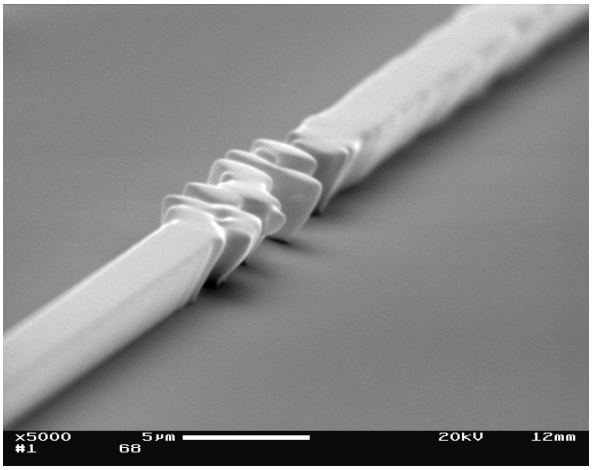


Figure 4.9: High dark erosion as a result of a poor softbaking at 100 °C for 45 s (AZ nLOF 2070 5:1 PGMEA resist on Si) [a]

[a] SEM measurement were carried out by using a ZEISS DSM942 Scanning Electron Microscopy

variations are even more evident when a non circular[4] geometry of wafer is spin coated. This is another advantage by using a circular 1" diameter wafer in the case of BF®33. Since this thickness difference on edges might affect spatial resolution during exposure, and a non-contact lithography may proceed, this should be avoided. After soft-bake I removed the edge of every sample by employing spin coater and isopropanol in the following way. I held the sample spinning at 2000 rpm and applied a fine stream of isopropanol on the edges of samples for 40 s. Then I dried the sample by utilizing a N_2 gun. Further results as well as corresponding endeavors to optimize soft-bake values are discussed in Section 4.3.6.

4.3.3 Exposure Dose

Exposure dose D is calculated by multiplying output intensity I from the mask aligner and exposure time, $D = I \cdot t$, in mJ/cm^2, where t is the time in seconds which the resist is exposed with. Mask aligner, with a Hg lamp of 350 W, in Uni Süd cleanroom facilities, provides an output intensity of 10,2 mW/cm^2.

Exposure dose is strongly dependent on resist film thickness (FT) and post-exposure bake (PEB). Sidewall profile depends on optimum exposure dose, whereas low exposure doses produce narrow lines and maximal undercut, high exposure dose do a weak or nearly no undercut (25). Low exposure doses produce that

[4] in case of Si wafers they are squares

substrate-near region of the resist remain poorly exposed, in consequence this region undergoes a high development rate and ends in a pronounced undercut. On the other hand, high exposure doses provide a more homogenous absorption of light through the resist, producing a weak undercut. On the extremes, too low and too high exposure dose are possible. However, in most of the cases non-desired results turn out by using one of them. In the first case, when too low exposure doses are used, the resist starts thinning and possible shortcuts during development might be observed. An exposure dose too high illuminates nominal dark resist parts by way of scattering, diffraction or reflection. Though, overexposure of the resist widens gap lines, one can take advantage of this. Particularly in this work wider gap lines than designed ones are obtained by adjusting development cycle.

From what is previously discussed, we do know optimized parameters for exposure dose should be attained for each size thickness and each linewidths. In order to find the right exposure time for each thickness different exposure series are performed by patterning the structures on Si wafers[1]. After achievement of a considered optimized value the structures are patterned on Au/Cr/BF33 wafers starting with final parameter regarding Si wafers. These series allow us to study in an easy way sidewall profile of the developed resist since Si wafers are simpler to cleave. Small variations in exposure time force to reoptimize exposure parameters on Au/Cr/BF33 wafers. As we have early discussed, reflectivity or transparency of wafers surface might change the optimum exposure dose regarding to Si wafers, however no critical difference between Si and Au/Cr/BF33 wafers is observed. Results from this exposure series are uncovered in Section 4.3.6.

4.3.4 Post-Exposure Bake

In addition to soft-bake, a further bake might be applied in some types of resist to improve mainly sensitivity in areas exposed by UV light. Since this bake is made posterior UV exposure, it is correctly named as post-exposure bake (PEB). This bake is performed to catalytically enhance and complete photoreaction initiated during exposure in the chemical amplified AZ® nLOF 2070 resist (25). It is

[1] Si wafers are easier to cleave than glass wafers

also fundamental for the crosslinking mechanism started during exposure. I take advantage, in some cases, that giving long PEB to AZ® nLOF 2070 resist a widening of exposed lines is observed. Beyond it could be a disadvantage during fabrication, by adjusting development cycle outstanding results to enlarge desired lines are possible. As it is properly explained in section 4.3.6, remarkable results are found by placing the samples on a hotplate for 1-3.5 minutes depending on resist thickness.

4.3.5 Development

After exposure and PEB of the AZ® nLOF 2070 negative resist, its dissolution in the unexposed areas increases when it is dunked in an aqueous alkaline developer. Contrary, if a negative resist is employed exposed areas are dissolved and unexposed parts remain after development. The development rate depends on both the resist and developer type. Special care should be taken by considering the compatibility between resist and developer −no critical in our case but− as well as substrate compatibility.

While accomplishing of development the carboxylic acid formed during exposure is moved from the hydrophobic to hydrophilic part of the cresol chain. It promotes the deprotonisation of the OH-group increasing the resist solubility in aqueous alkaline developers. Besides carboxylic acid, acetic acid formed by alkaline developers from the resist solvent PGMEA also increases the resist dissolution rate.

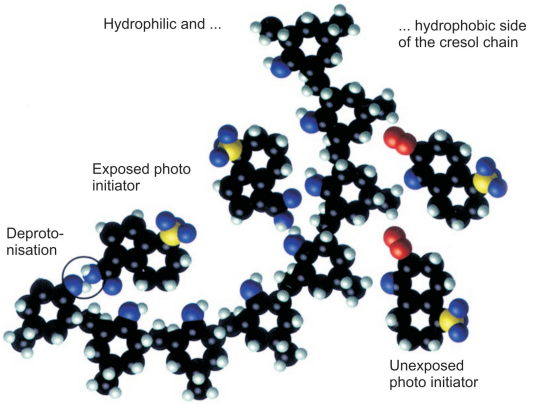


Figure 4.10: Development mechanism of photoresist (25)

AZ® 826 MIF[1] is a compatible developer to AZ® nLOF 2070 negative resist. This developer is produced by and purchased from Microchemicals. It is an organic developer based on TMAH[2], which is used where mobile ions like Na^+ are of interest. AZ 826 MIF is based on 2.38 % TMAH and prepared to maximal standards, it also contains different surfactants for higher dissolution rates and residue-free development.

Development process is performed as follows. Two beakers are placed on a water bath at 23 °C, the first one containing ∼20 mL AZ® 826 MIF, and the second one having ∼20 mL of deionized H_2O. The post-exposed and photopatterned resist is soaked in the beaker which contains the developer AZ 826 MIF

[1] Metal Ion Free
[2] tetramethyl-ammoniumhydroxide

for some minutes[1]. After proper development time, the sample is soaked and gently stirred in a beaker containing deionized water for 20 s. Subsequently, the sample is removed from water bath and, since some developer might remain after development, the sample is rinsed with plenty of water.

Without changing other previous parameters (exposure dose, soft-bake, etc.), it is observed that the thicker the resist layer the longer the development time is necessitated. For resist thick layers (FT $> 3\,\mu$m), an optimization for each thickness should be done (25). By fixing preceding parameters I found that an optimum development time of 1 min and 50 s for a resist thickness within 3-4 μm is required. Others values regarding thickness size are completely detailed in next section.

4.3.6 Lithography Output

Up to now parameters that evidently influence lithography output have been separately explained. Since association within each other is unavoidable this section intends to elucidate what optimization of each parameter brings out.

Optimization on Si

To start optimization of photolithography parameters I decided to fix resist thickness, soft-bake, post-exposure bake and development time aiming a variation of exposure dose. As a methodical selection during whole thesis both soft- and post-exposure baking time maintain the same value, and only change when resist thickness does. First planned temperatures are as suggested by Microchemicals both soft-bake and post-exposure bake at 110 °C. Corresponding parameters from this first exposure series appear in Table 4.3.

The mask employed to carry out this exposure series has an array of different crossing lines and widths varying within 0.5-2.0 μm. The substrate for these samples is Si, since a cleaving process is suitable for studying cross section of developed resist. By means of an optical microscope, with a maximal magnification of x100, I observed each of the samples immediately after development cycle. The corresponding parameters to them are displayed in Table 4.3. Also by inspection

[1]Specific information is found in section 4.3.6

Table 4.3: First exposure dose series of diluted 5:1 AZ® nLOF 2070 resist. These table indicates that by varying exposure dose and holding fixed the other parameters a possible optimization could be attained

SB[a] [°C, s]	ED[b] [mJ/cm^2]	PEB[c] [°C, s]	DC[d] [s]	FT[e] [μm]
110, 60	77.40	110, 60	60	3.3
110, 60	56.10	110, 60	60	3.3
110, 60	**45.90**	**110, 60**	**60**	**3.3**
110, 60	40.80	110, 60	60	3.3

[a]Soft Bake
[b]Exposure Dose
[c]Post Exposure Bake
[d]Development Cycle
[e]Resist Film Thickness

through optical microscope I determined those samples having linewidths closer to mask design. In this respect, I found that when resist is exposed with 45.9 mJ/cm^2 finest result are obtained. Figure **??** indicates that, when lines are separated by the same width, linewidth = spacewidth, development time seems to be not enough. However, if lines are not closed each other well developed lines are obtained and they show an undercut profile as it is depicted in further pictures in Figure **??**. By slightly scratching on one side of the Si substrate, with the help of a diamond tip, I cleaved the sample and studied its cross section as it is shown in Figures **??**b-d. As we can observe a visible undercut results from this sample, which might be caused either by a long development time, short post-exposure bake or overexposed dose. Nevertheless, they reflect a negative slope profile, which is desirable in the case of lift-off process as it is suggested by Microchemicals Inc.

Instead, since the fabrication outline required an electroplating process an nearly vertical and smooth sidewall profile is sought. From resist datasheet is advised that if we pursue a smooth sidewall profile, a difference of 20 °C, between soft-bake and post-exposure bake, must be practiced. In that case, a second exposure series is used up and it is represented in Table 4.4. As well as foregoing

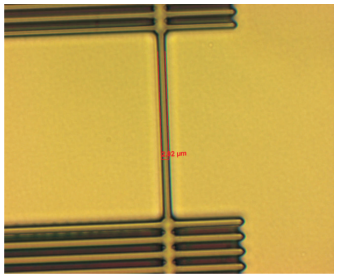
samples they are spin coated on Si wafers. As we can watch from this table both soft-bake and post-exposure baking temperature in addition to resist thickness have been changed. Exposure series is started with preceding optimal exposure value of 45.9 mJ/cm^2 and after varied.

Table 4.4: Second exposure dose series of diluted 5:1 AZ® nLOF 2070 resist. In this second exposure series, the soft- and postexposure bake have been modified with respect of first series. The tendency says that lower exposure dose are required to achieve optimized results.

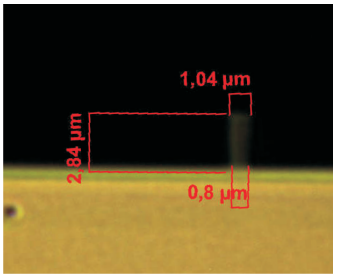
SB [°C, s]	ED [mJ/cm^2]	PEB [°C, s]	DC [s]	FT [μm]
100, 60	45.90	120, 60	60	2.8
100, 60	30.66	120, 60	60	2.8
100, 60	20.40	120, 60	60	2.8
100, 60	**17.34**	**120, 60**	**60**	**2.8**

By having a look trough optical microscope of each sample I found out that best results are attained when resist is exposed with 17.34 mJ/cm^2, as Figure 4.11 screens. This lower exposure dose is understood in the following way. Since post-exposure temperature has been increased the sensitivity to crossliking under UV light of the resist does as well. This brings us out that, as a result of higher PEB, less exposure dose and vertical-like sidewall profile are acquired. As consequence of having less exposure time, the possible standing waves of the light due to diffraction are diminished, giving a smoother sidewall surface. On the other hand, vertical-like sidewall profiles are wished for optimal operation of surface-electrode ion trap. Figure 4.11a, as encountered in Figure **??**, also reveals underdevelopment when spacewidth is the same as linewidth. This picture clearly bares that a longer time during development must be procured. For this reason a development series is run by holding the other parameters unceasing.

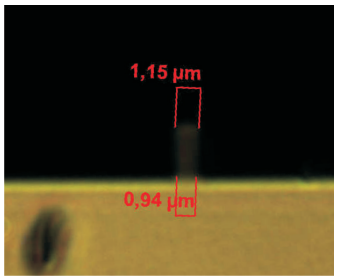
The two aforementioned exposure series harvest that a longer development time is necessary. Under this purpose, I made a sequence of samples in such a way that only variation of development cycle is considered, as it is indicated in Table 4.5. High-quality results are shown by a sample developed for 110 s.



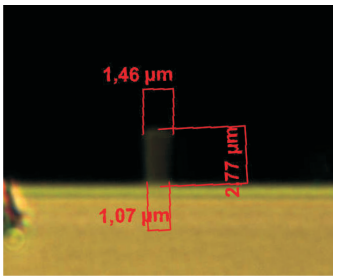
(a) 2.0 μm underdeveloped lines



(b) 1.0 μm (top) and 0.8 μm (bottom)



(c) 1.1 μm (top) and 0.9 μm (bottom)



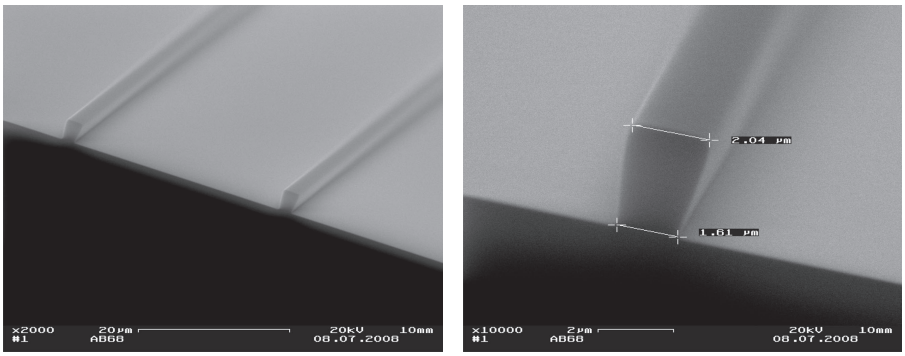
(d) 1.4 μm (top) and 1.0 μm (bottom)

Figure 4.11: After second dose exposure series the exposed 5:1 AZ® nLOF 2070 resist, with 17.34 mJ/cm^2, shows an aspect ratio about 3:1

Table 4.5: Development series of diluted 5:1 AZ® nLOF 2070 resist. Prior exposure dose series indicated a development series was mandatory. In this series, the development time in incremented from 80 s to 115 s while holding constant the rest of parameters.

SB [°C, s]	ED [mJ/cm^2]	PEB [°C, s]	DC [s]	FT [μm]
100, 60	45.90	120, 60	80	2.8
100, 60	45.90	120, 60	90	2.8
100, 60	**45.90**	**120, 60**	**110**	**2.8**
100, 60	45.90	120, 60	115	2.8

This sample is exposed by occupying the ion trap mask design and the structures resulted from photolithography are enacted under SEM studies, as paraded in Figure 4.12. These latter studies reveal a slope angle around 86° by measuring top and bottom cross sections of the resist lines.



(a) RF-GD-RF electrodes space (b) 86° sidewall negative slope

Figure 4.12: The resist mask shown in these pictures was achieved with a development time for 110 s in AZ® 826 MIF, previously exposed during 45.90 mJ/cm^2 with a soft-bake at 100° for 60 s and a post-exposure bake at 120° for 60 s.

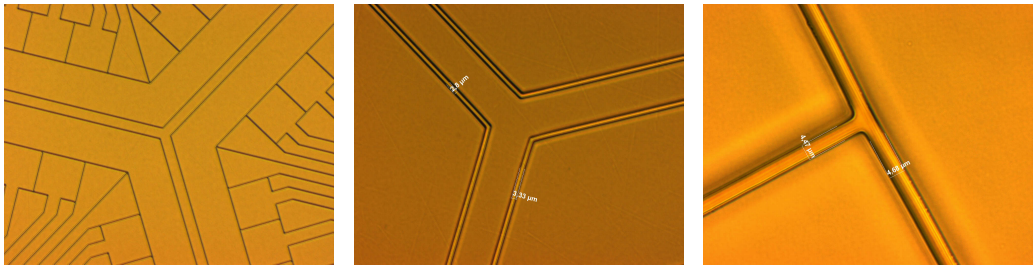
Optimization on Au/Cr/BF33

According to photolithography outcomes on Si wafers I decided to pattern the mask resist on Au/Cr/BF33 wafers by drawing on surface-electrode mask design. Further results are shown and related as follows. Due to the results found in Table 4.5, I decided to pattern the diluted 5:1 AZ nLOF resist by employing surface-electrode mask design on Au/Cr/BF33 wafers. A diminished soft- and post-exposure baking time for 45 s is selected intending to bring out better results during electroplating process. Furthermore, from now till end, I refer to these samples with the assigned labels in Table 4.6. Along next fabrication steps, succeeding results are demonstrated and discussed.

Table 4.6: Photolithography parameters for chips achieved by using a 5:1 AZ® nLOF 2070 negative resist. The spin coating was carried out by using 4000 rpm.

Chip	SB	ED	PEB	DC	FT	Linewidth	
						Resist	Mask
	[°C, s]	[mJ/cm^2]	[°C, s]	[s]	[μm]	[μm]	[μm]
1	100, 45	38.76	120, 45	110	3.3	1.85	1.4
2	100, 45	34.86	120, 45	110	3.3	1.47	1.4
3	100, 45	41.82	120, 45	110	3.3	2.10	1.4

At first, for Chip 1 and Chip 3, the alignment of mask is made in such a way that lines of 1.4 μm from the surface-electrode mask design are hoped for. After exposure of Chip 1, developed resist endures overexposed lines as consequence of a high exposure dose of 38.76 mJ/cm^2, which widens developed structures on top and thins on bottom. These results suggest to decrease exposure dose, as it is done for Chip 2, where a visible improvement is obtained when I expose with a value of 34.86 mJ/cm^2. Its developed structures are shown in Figure 4.13a and the linewidth is about to 1.47 μm which is measured after electroplating by means of SEM. A third chip is exposed by using an exposure dose of 41.82 mJ/cm^2. These last three chips are suitable for electroplating process since they exhibit no visible dirt or holes or high dark erosion that might cause any shortcut between plated electrodes. However, only Chip 3 sustained the rest of the process until



(a) Center of the resist mask of Chip 2 (b) Resist mask of Chip 4 (c) Chip 6

Figure 4.13: Different parts of the surface-electrode resist structure are shown. All samples sustained a deevelopment time for 110 s in AZ826 MIF and the other corresponding photolithography parameters are found in Table 4.6 and 4.7.

it could be tested for electrical breakdown as it shall be shown in Chapter 5. In the case of Chip 1, any further step after trials for Au etching were possible. Specific information is found in section 4.6. On the other hand, Chip 2 presented complications when I made ultimate step, Cr etching, since adhesion layer could not be removed as it is explained in section 4.7. As it happens, these latter "errors" are the preamble of the first successful chip, Chip 3, since a completion of all fabrication steps is fully attained by improving parameter used in previous, Chip 1 and 2, as they are examined along the rest of fabrication steps.

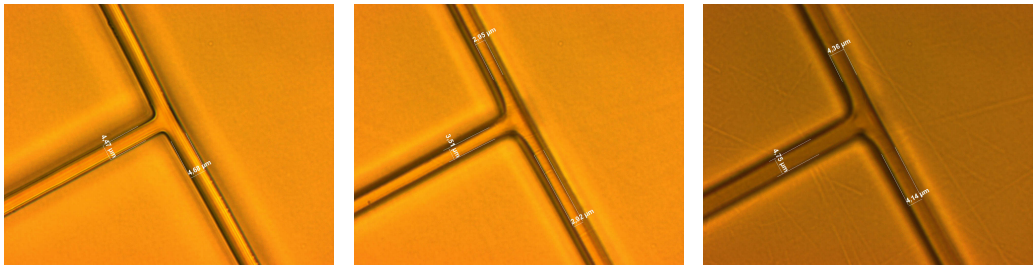
Table 4.7: Photolithography parameters of AZ® nLOF 2070 negative resist. The corresponding spin speeds that provide the resist thickness on these samples can be red from Figure 4.8.

Chip	SB	ED	PEB	DC	FT	Linewidth	
						Resist	Mask
	[°C, s]	[mJ/cm^2]	[°C, s]	[s]	[μm]	[μm]	[μm]
4	100, 90	159.12	120, 50	220	6.0	3.10	2.6
5	100, 90	159.12	120, 70	220	6.0	4.00	2.6
6	90, 120	236.64	110, 120	220	9.2	4.68	2.6

Electrical breakdown results, which are described in Chapter 5, advise that

a larger inter-electrode gap to fulfill the theoretical demands for ion trapping is required. Within this context, two more chips are prepared and are depicted in Table 4.7, and labeled as Chip 4 and 5. Corresponding wafers to samples showed in Table 4.7 are spin coated with a non-diluted AZ® nLOF2070 resist in order to get a 6.0 μm resist thickness. By doing a exposure series, as developed at the beginning of this section, I found suitable parameters are the ones belonged to Chip 4 in Table 4.7. However, the larger the inter-electrode gap the better the electrical breakdown performance is expected. Thus, I decided to increase post-exposure baking time intending to gain wider structures. Those results are evidently revealed by Chip 5 where compared to Chip 4, a longer post-exposure baking time allows to increase inter-electrode gaps from 3.1 to 4.0 μm. These results as previous ones, once again, confirm that widening of linewidths are feasible by tuning exposure dose and post-exposure bake values. As I have remarked in earlier sections, it is of underlined importance that sidewall profile are held as vertical as possible. Although shielding of static field caused by the presence of substrate is low when an aspect ratio is about to 1, it is ideal if a larger aspect ratio is purchased. Even final Chips 4 and 5 attain such appropriate aspect ratio I decided to prepare a final Chip with a highest aspect ratio about to 2. This sample is labeled as Chip 6 and is the most successful chip made in this work. As I have beforehand indicated a exposure series prior to pattern on Au/Cr/BF33 are carried out in order to obtain best parameter for a resist of 9.0 μm linewidth, former results show that most suitable parameters are those bared by Chip 6. The posterior sidewall profile of the inter-electrode gaps for this sample are expected, as represented by defocus in Figure 4.14, to be round negative. These profile is achieved by reducing the development time in order to avoid a undercut sidewall profile.

The samples shown in Table 4.6 and 4.7 are sustained to electroplating process. Particularly, Chips 3 and 5 are successfully employed for electrical breakdown as it is explained on Chapter 5. On the other hand, Chip 1, 2 and 4 undergo along certain fabrication step some problems that shall be detailed in the ensuing fabrication steps. Lastly, a last sample, Chip 6, with an aspect ratio 3:2 is fabricated and operated under high vacuum conditions. Supplementary information about Chips 3, 5 and 6 are given in the following sections.



(a) Top 4.68 μm (b) Middle 2.95 μm (c) Bottom 4.10 μm

Figure 4.14: A defocus series which depicts the diffrence in thickness of the developed resist mask attained for Chip 6 with the photolithography parameters displayed in Table 4.7.

4.4 Electroplating

To grow gold layer in the space between mask resist (developed resist structure) one has to entail the usage of a deposition method. Electroplating reveals more advantages than other methods, such as evaporation and sputtering, as compared in Chapter 4.

Table 4.8: Voltage, current, as well as plated gold thickness are shown. The reduction of the voltage is intended to achieve a improve homogeneous Au growth.

Chip	Current [mA]	Voltage [V]	Plating [μm]
1	0.80	0.48	1.98
2	0.84	0.45	2.10
3	0.80	0.28	3.0
4	0.86	0.30	4.0
5	0.80	0.30	4.6
6	0.72	0.25	6.2

As it has been explained in section 4.2, a Au seed layer of 50 nm is built up on top of Cr/BF33 substrate. I patterned these substrates containing a seed layer with the parameters shown in Tables 4.6 and 4.7 as it is explained in section 4.3.6.

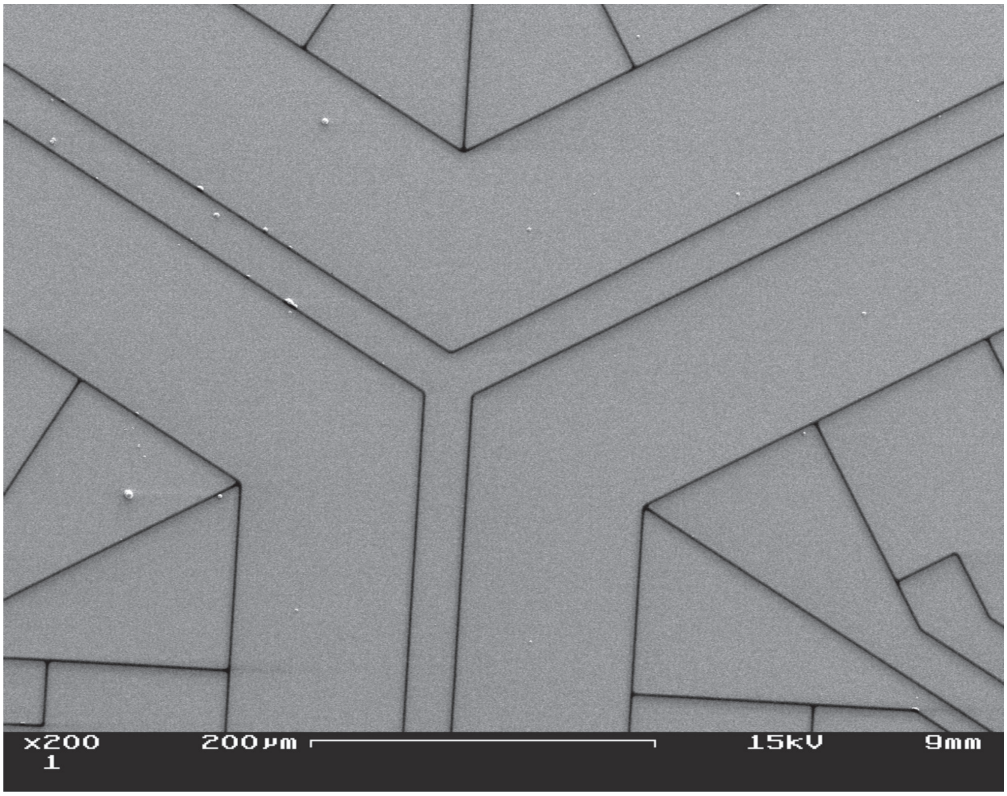


Figure 4.15: SEM image bares the center of Chip 1 after electroplating. The resist mask appearing in dark lines sustained electroplating bath.

Electroplating process is carry out by MicroGan GmbH (www.microgan.de) and corresponding plating parameters are displayed in Table 4.8. Original results as exhibited in Figure 4.15 present protuberances (small white dots) on plated surface. They are due to a high voltage employed during deposition. In order to dimmish those protuberances, and to increase layer homogeneity for next chips, the voltage has been reduced from 0.48 to 0.25 V. Best results for surface trap are obtained by reducing such voltage as we see in SEM pictures in the following sections.

4.5 Stripping of Resist

After photolithography and specifically after electroplating, resist mask should be completely removed from wafer. NMP is a good choice due to its outstanding physical properties. Among them, some important are that: i) NMP yields a low vapor pressure, which causes a slow drying and thus there is no re-deposition of stripped photoresist onto the substrate which avoids striation formation, ii) NMP also strongly dissolves organic impurities as well as resists, keeping the removed resist in solution, and being able to heat it up to 80 °C due to its high boiling point thus improving the performance.

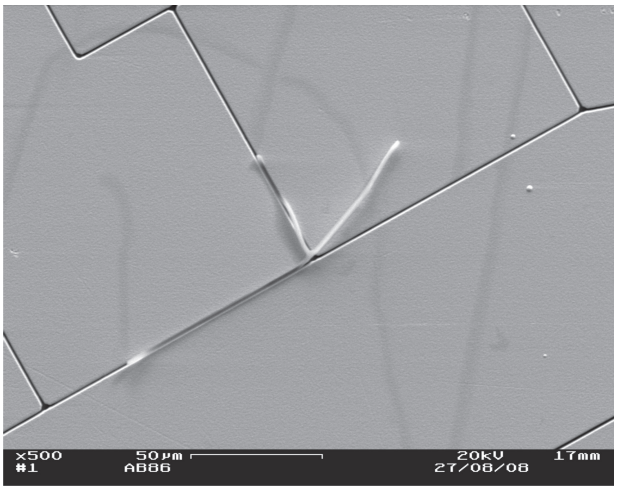


Figure 4.16: Chip 1 was immerse in a 20 mL solution of NMP for 36 h at room temperature. After stripping process by using NMP evident resist residues stand inside inter-electrode trap. Thus a dry cleaning process by means of $RIEO_2$ is suggested.

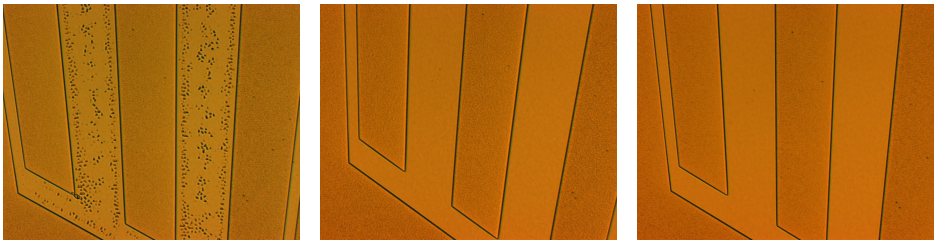
Nevertheless, once AZ® nLOF 2070 resist is exposed by UV light, a dissolution, intended by using a solvent such as acetone or NMP(1-Methyl-2-pyrrolidon) is rather complicated. Therefore, a stripping of resist is performed by lifting off the resist mask from substrate and sustaining the sample under $RIEO_2$.

Earlier trials for stripping process of Chip 1 is ensured by immersing the sample in 20 mL of NMP for 36 h without any high-quality result as it is depicted in Figure 4.16. SEM image certainly displays a part of mask resist that is not totally removed.

A second trial is carried out by pouring Chip 3 in NMP for 29 h, and two steps, 5 min and 15 min, under $RIEO_2$. No difference between 29 h and 36 h is found, but $RIEO_2$ seems to be more effective when some resist residues remain

on chip. A stripping series exposing the results of these latter steps are put on view in Figure 4.17.

A final trial by soaking chips in NMP for 2 h and then two steps of 10 min under $RIEO_2$ brings us supreme results. No residues of mask resist are found as it is depicted by SEM image in Figure 4.18 for Chip 4. This last optimums stripping process is applied on the rest of chips, Chip 5 and 6.



(a) 29 h NMP (b) $RIEO_2$ for 5 min (c) $RIEO_2$ for 15 min

Figure 4.17: Chip 3 is soaked in a 20 mL solution of NMP for 29 h, after which there still exist resist residues. A first cleaning step by employing $RIEO_2$ etching means for 5 min presented a visible improvement. A further 10 min by using $RIEO_2$ was carried out an effective resist removal was accomplished.

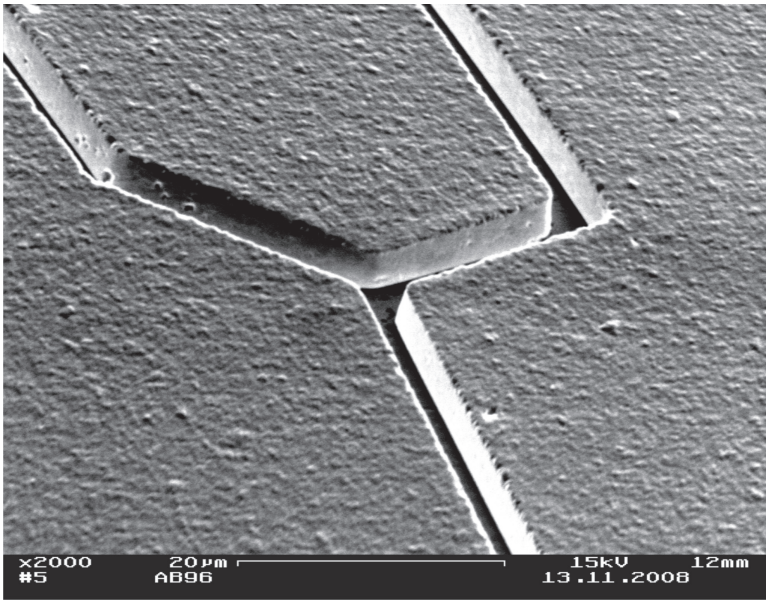


Figure 4.18: This SEM micrograph corresponds to Chip 4 after 2 h in NMP and 20 min in $RIEO_2$. By employing 20 min in an atmosphere of O_2 it is demonstrated that fully stripping of resist is attained. No resist residue under SEM studies were found. The results by utilizing long time in $RIEO_2$ guarantee a successful wet etching of Cr/Au layer.

4.6 Gold Etching

Gold is a transition metal and can form trivalent and univalent ions upon solvation. Au has a FCC (face-centered cubic) crystal structure and its density is 19.3 $g \cdot cm^{-3}$. Its fully occupied 5d orbital, in its electron configuration $[Xe]4f^{14}\,5d^{10}\,6s^{1}$, extends outside the single valence electron from the 6d orbital. This prevents or make difficult any oxidizing reaction.

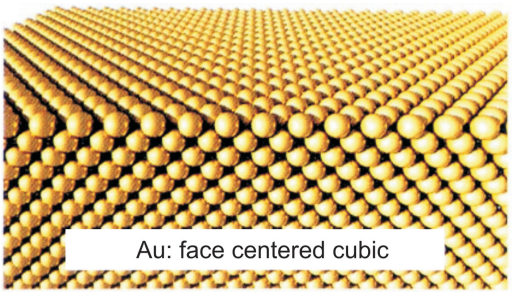


Figure 4.19: FCC gold structure. Taken from (25)

As a result, wet etching of Au requires a strong oxidizer for the separation of single electron valence, in the same manner a complexing agent which overwhelms the reassembly of oxidized gold atoms back into the solid (25). Typically, a so called *agua regia*, a mixture of nitric acid and hydrochloric acid, is used under this purpose. This mixture, which regularly is done in a mixing ratio 1:3, is able to etch gold at room temperature.

As it has been exlplained in section 4.2 that a 50 nm starting layer of Au is a prerequisite to attain successful results during electroplating. After striping of resist the Au starting layer should be removed in order to accomplish insulating inter-electro gaps. The Au starting layer is selectively etched by using Iodine/iodide (KI/I_2) solution where Gold and Iodide form gold iodide (AuI) as follows:

$$2\,Au + I_2 \rightarrow 2\,AuI \tag{4.2}$$

By adding KI to the solution the solubility of AuI is increased. KI/I_2 used in the cleanroom facilities shows an etch rate about 16 nm/min. Original attempts to understand Au etching as well as etching rates are performed on Chip 1 using this etchant. This chip was immersed in 10 mL of KI/I_2 for 220 s (11 steps of 20 s). Within each step the chip is dried by utilizing N_2 gun, acetone and water, the sample is characterize under optical microscope. A series of pictures of selected

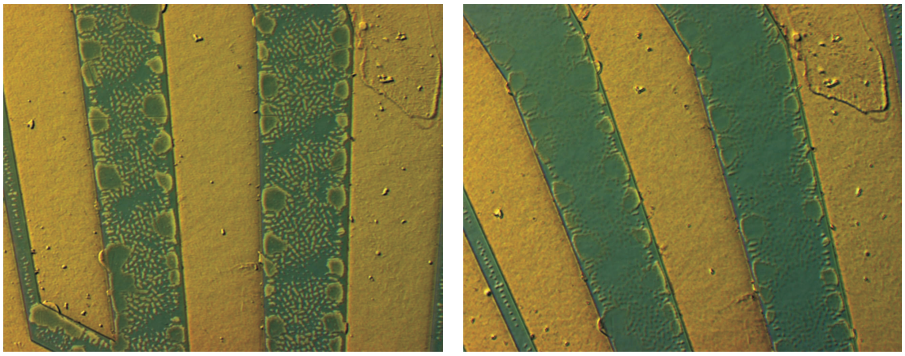
steps are disclosed in Figure 4.20 where a diminish in reflectivity is observed which indicates the roughness of the etched surface has increased.

Moreover, SEM studies are performed to understand whether Au has been properly etched or not. These pictures are disclosed in Figure 4.21, as we can observe an evident roughness in addition to remained gold within inter-electrode gaps. The increment in roughness is due to: i) inhomogeneous etching rates are caused by the presence of acetone residues, acetone residues might create preferential etching zones thus acting as mask during etching, ii) it is possible that etching rate is too high that larger areas are etched faster than small ones. After this trial on Chip 1, any other further step could be possible since remained gold create connections between electrodes.

Due to these results, next trial on Chip 2 is intended where acetone is not applied anymore. In this case, instead of doing intermediate steps during the etching process this is done in one puddle of 3 min and 20 s. Outcomes from this trial is depicted in Figures 4.22 and 4.23. Although seed layer is fruitfully etched away, there is a manifest roughness, even on sidewalls, which is not desirable for ion trap tasks. Thus I decided to dilute KI/I_2 in H_2O, with a solution proportion of KI/I_2 : H_2O = 1 mL : 2 mL. This dissolution provides a lower etch rate of 4 nm/min.

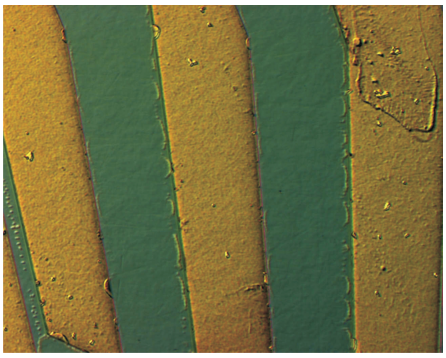
A test with this new etching rate is undergone by Chip 3 in the following way. The sample is soaked in three puddles of diluted KI/I_2. The first one, for 7 min and 20 s, a second one for a 1 min and final one for 1 min and 40 s.

From results of Au etching of Chip 3, I decided to etch Chip 4 and afterwards Chip 5 and 6 in this manner. Chip 4 is immersed in diluted KI/I_2, by using five puddles, 3 of them for 3 min, a fourth for 2 min, and a final for 1 min after Cr etching. In total, a etching time of 12 min is needed to completely removed Au seed layer. In Figure 4.24 a sequence of part of Chip 4 is disclosed showing the evolution during etching time of the seed layer removal.

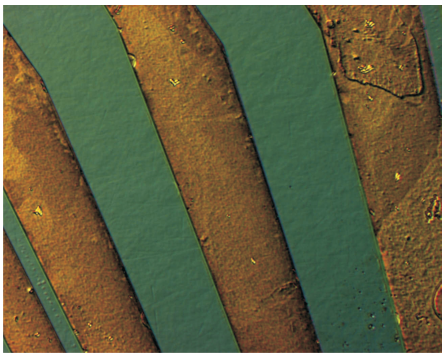


(a) 60 s

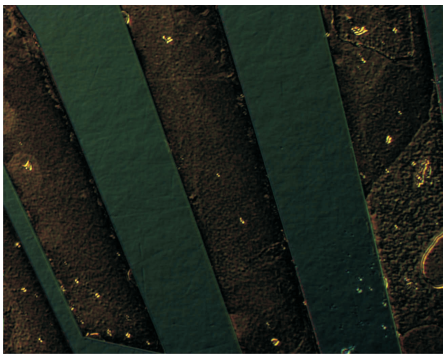
(b) 80 s



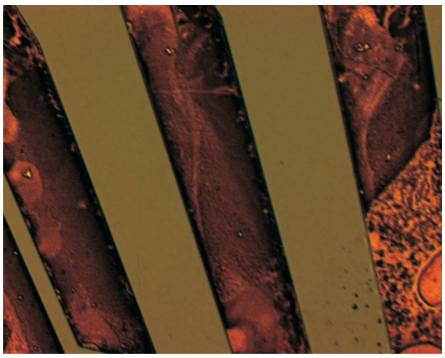
(c) 100 s



(d) 120 s

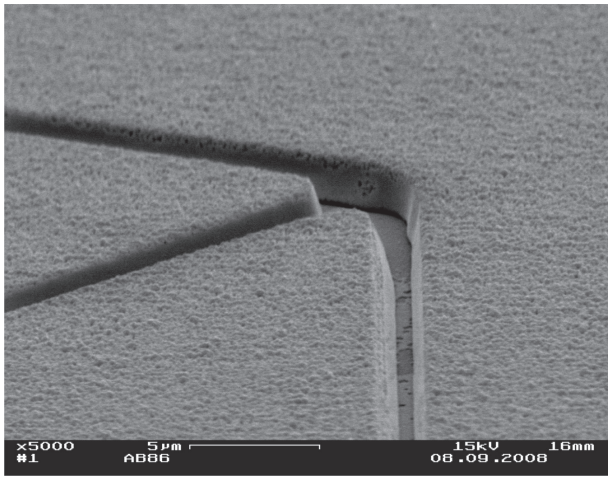


(e) 140 s

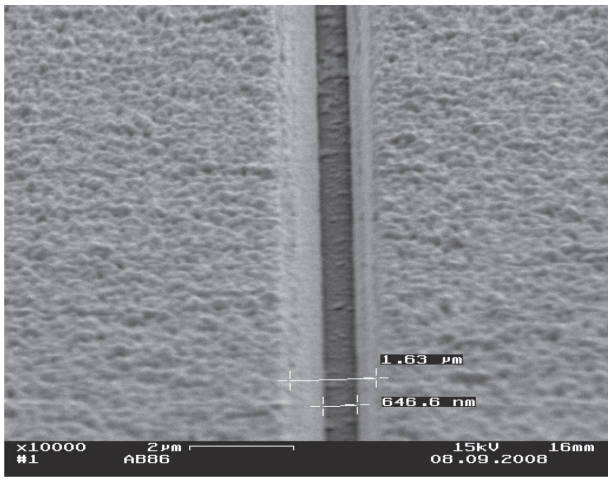


(f) 180 s

Figure 4.20: A etching time sequence is performed in order to determine the etch rate of the Iodine/iodide (KI/I_2) solution. As the pictures series display the longer the gold structure is immerse in the etchant a visible degradation of the gold surface is observed, by comparison of reflected light. Thus, it shows the importance of utilizing the minimum Au seed layers thickness to avoid an increment of surface roughness when longer etching times are performed. This pictures correspond to Chip 1 which was patterned with 17.34 mJ/cm^2 in a diluted 5:1 AZ® nLOF 2070 resist, and shows an aspect ratio for patterned structures about 3:1



(a) 80 s



(b) 180 s

Figure 4.21: The gold structures depicted in Figure 4.20 were studied under SEM measurements. From this pictures a evident surface roughness appeared as a result of the fast etch rate presented by Iodine/iodide (KI/I_2) etchant solution and the use of solvent during the process. It is believed that solvent residues creates preferential etching site which undergo faster etch rates when compared with non-preferential. Thus, it results in an evident increase of surface roughness. From this results I decided to reduced the concentration of the etchant in the solution by diluting it in H_2O, and prevent the use during etching process of any solvent. The etching process is stopped by immersing the sample in a beaker with water. The corresponding proportions are given below.

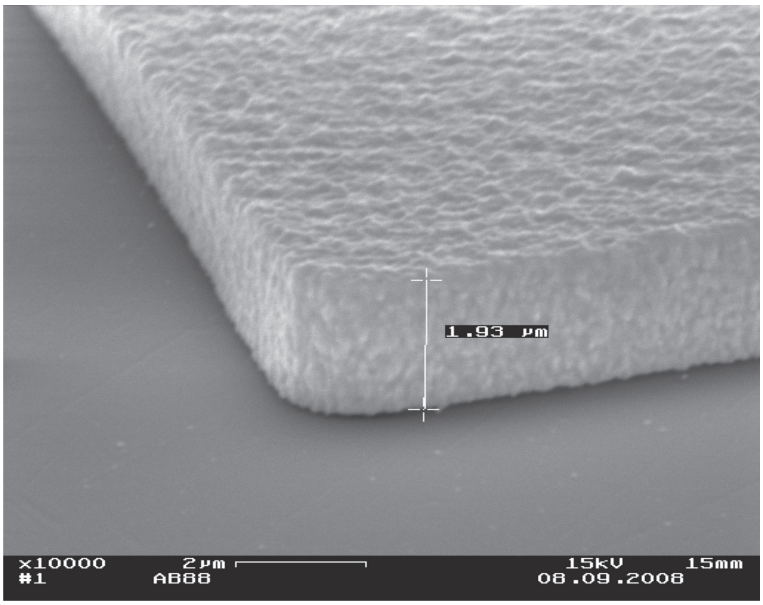


Figure 4.22: For Chip 2 a dilution of gold etchant KI/I_2 : H_2O = 1 mL : 2 mL was selected which showed a visible improvement in surface roughness when we observed it through scanning electron microscopy.

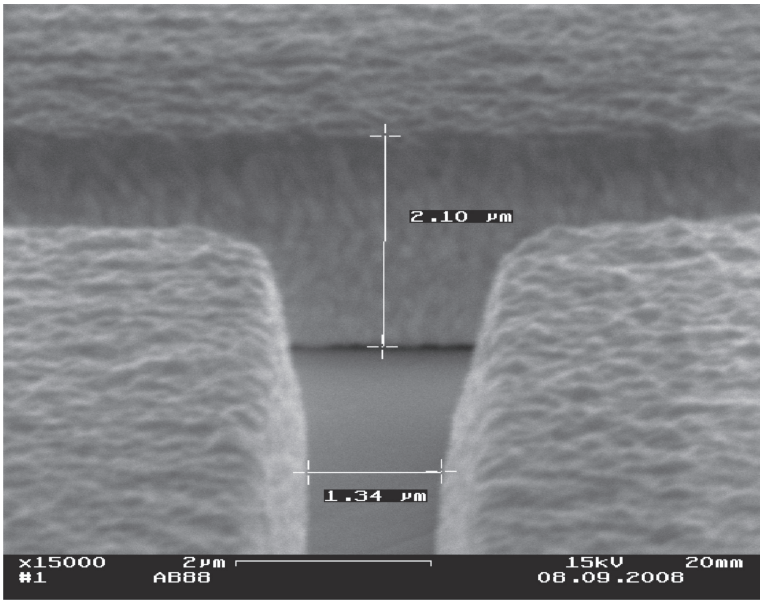
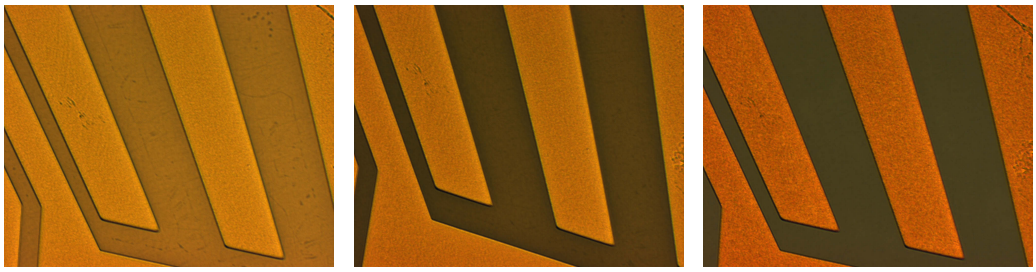


Figure 4.23: After proper Au etching the aspect ratio of the plated Au electrodes was measured on Chip 2. The SEM micrograph displays an aspect ratio near to 2. Which might guarantee shielding of static field produced in the insulating gaps when trap be operated.



(a) 3 min (b) 6 min (c) 11 min

Figure 4.24: For Chip 5 an Au etching optimization by using diluted IK/I was employed. A sequence of pictures after determined time period were taken and compared until no visible gold on large gaps was observed. When the etching time undergo around 11 and 12 min there is no observable change in the color of the large gaps which suggest all gold has been etched.

4.7 Chromium Etching

During fabrication an intermidiate layer with finest adhesion properties is required to avoid any peel off from Au electrodes. At the same time a material with feasible wet etching characteristics is mandatory. Chromium (Cr) is a hard metal with stupendous adhesion properties to many materials. In this sense, under the scope of our macrofabrication process Cr is selected as the adhesion promoter between BF® 33 and gold starting layer.

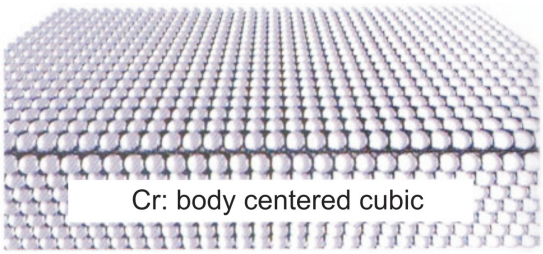
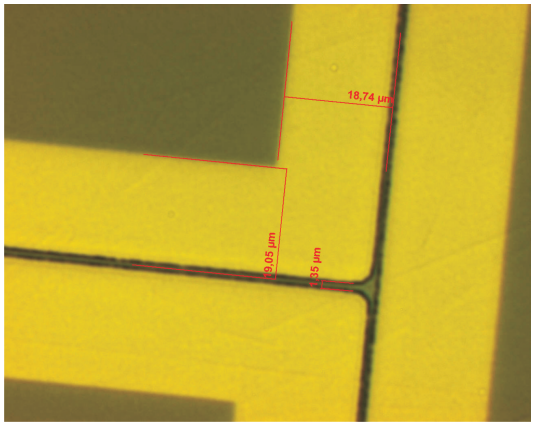


Figure 4.25: Chromium structure. Taken from (25)

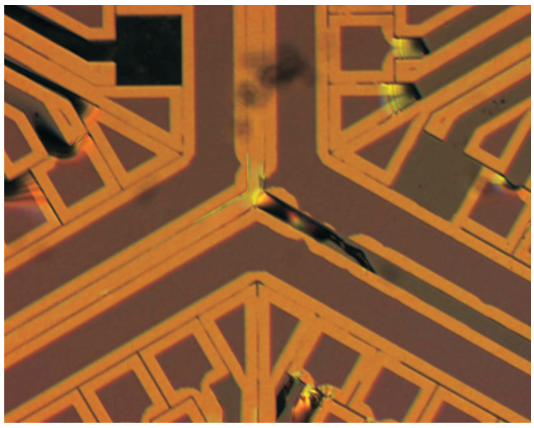
After Au etching an additional Cr etching step should be done in order to finally achieve a good electrical insulation within Au electrodes. Required Chromium etchant, "Chromium etchant No. 1", is purchased from Microchemicals Inc. which has the following composition: Ceric ammonium nitrate : perchloric acid : H_2O = 10.9 % : 4.25 % : 84.85 % and reveals an etching rate of 600 nm/s at room temperature.

I soaked the Chip 1 in 10 mL of chromium etchant No. 1 for 30 s and a visible underetch is observed. Through optical microscope means and facing down the sample I have a look the etching range and as it shown in Figure 4.26 it overtakes up to 20 μm beneath Au electrodes. This underetching produced that many of the electrodes were lifted off, which spoiled this chip for further steps such as electrical breakdown.

On the other hand, the fast etching rate originally observed in Chip 1 earlier samples suggested to lower this high rate. A convenient dissolution in water with the solution proportion Cr etchant : H_2O = 1 : 2 is done which shows an etch rate of 100 nm/s. Etch time used for successful Cr etching lies between 10 and 12 s, as shown in Figure 4.27.

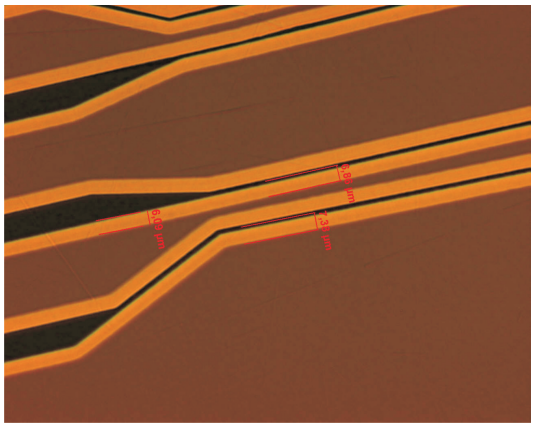


(a) Cr etching for 30 s

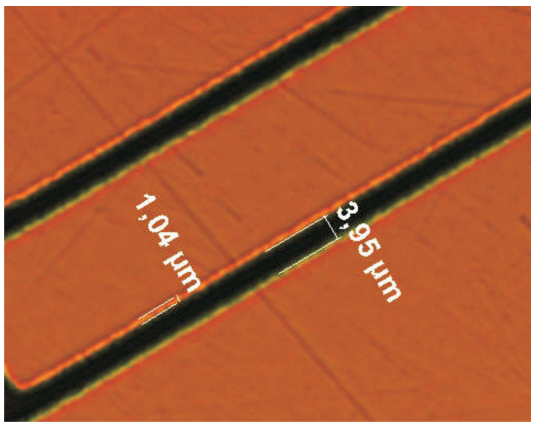


(b) Cr etching for 30 s

Figure 4.26: The fast etch rate original testen in Chip 1 underetched up to 20 μm of the adhesion layer. Due to this reason, some electrodes were peeled off, which inhibited any further step was possible.



(a) Using non diluted Cr. etchant for Chip 2



(b) Using diluted Cr. etchant for Chip 5

Figure 4.27: Chip 5 undergo etching time between 10 and 12 s, and it discloses a visible improvement of the underetched regions, when compared to Chip 2, where no dilution was proceeded.

4.8 Chip Dicing

Conventionally, a cutting or cleaving process might be done before a cleaning process of resist is carried out. However, most convenient cleaving process matching fabrication steps must be performed as an ultimate step.

I cleaved Chips 1, 2, 3 and 4 by utilizing a diamond tip. However, since most of the time this way of cutting the substrate is extremely risky I decided to employ for the important Chips 5 and 6 the workshop facilities in the west part of University of Ulm.

Thus slicing of Chips 5 and 6 is made in the workshop facilities at University West, where a dicing saw michine APD1 Logitech® is employed to achieve the require dimension of trap chip.

Basically, APD1 Logitech® is a combined annular and peripheral saw, this machine is computer-like controlled and is ideal for slicing samples such as wafers, crystals or semiconductor components up to 55 mm in diameter with minimal kerf loss or for precision dicing of wafers up to 100 mm (4") in diameter (**?**).

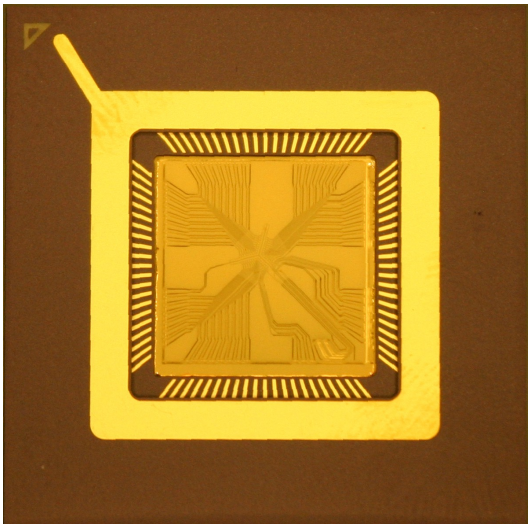


Figure 4.28: Kyocera chip carrier holding surface-electrode trap Chip 5 for electrical breakdown test

After dicing the diced chip is mounted placed in a 84 pins Kyocera chip carrier. The proper bonding for this microstructures is discussed in the next section.

4.9 Wirebonding

Microdevices require a proper bonding beyond conventional soldering due to their very small dimensions. A method of integrating chip-scale devices is called wirebonding which uses a combination within heat, pressure, electrical discharge and ultrasonic energy to weld chip-electrodes to chip-carrier pins.

The machine used to bond the chip electrode to the chip carrier pins is a HB10 Ball & Wedge Bonder (www.tpt.de) located in our QUELE laboratory. This bonder uses a combination of pressure, ultrasonic energy and heat to connect the chip electrodes to electrical supply by making a weld between the chip electrodes and chip carrier pins.

The common wires, usually are Au, Al or Cu, which have 25 μm in diameter, thus permitting many welds in a small area. The two most common modes of wirebonding are *wedge* bonding and *ball* bonding (26). When ball bonding, the 25 μm Au wire through a disposable tool called the capillary is fed. Then a high-voltage electric charge is applied to the wire. This melts the Au wire at the tip of capillary. Due to surface tension, when a electrical discharge is applied, a Au ball is create at the tip of the capillary. A clamp above bonder tip holds and moves precisely the Au wire whereas wirebonding. The ball rapidly solidifies, and the capillary is brought near to the electrode surfaces, which commonly are heated up tp 125 ° C. With the help of a tranducer the capillary is pushed down to electrode surface and by a conbination of heat, pressure and ultrasonic energy a weld between the Au electrodes and the Au gold is created. Although, there also is wedge bonding, in this experiments I have used only ball bonding mode to create the electrical connection for breakdown voltage test.

The ball wirebonding of the Chip 3 is displayed in the Figure 4.29. It is realized that this wirebonding mode permits that high-frecuency voltage may be applied to the electrodes.

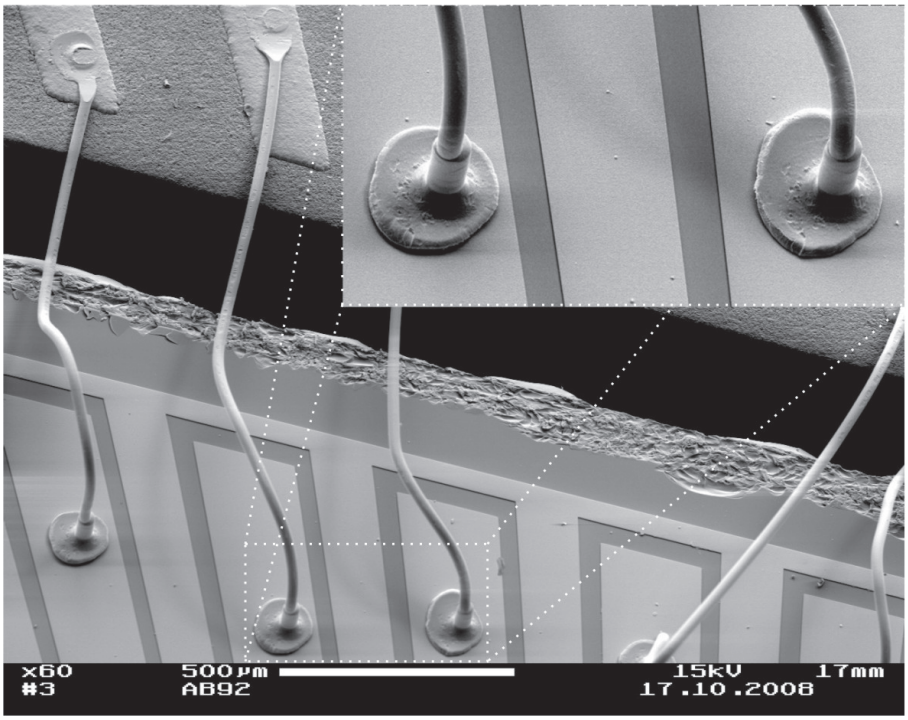


Figure 4.29: Ball wirebonding of Chip 3 by using 25 μm gold wires.

Chapter 5

Testing of the Microtrap Chip

I've got something you can never eat.

Marilyn Manson

This chapter involves the electrical breakdown test of Chip 3 and Chip 5. This chapter does not intend to explicate the phenomena involved behind electrical breakdown but looks for a quantitative measurement of the highest voltages to be applied for the corresponding inter-electrode gaps that are presented here.

5.1 Electrical Breakdown

To sustain the surface-electrode chips to the electrical breakdown test I built up the setup shown in Figure 5.1. It is arranged in the following manner. First of all, the chip is previously bonded by using ball bonding to a 84pin Kyocera chip carrier. The pins from the chip carrier are soldering to a PC Board (PCB) which allows a feasible manner to supply the high voltages inside the vacuum chamber. The vacuum enviroment is reached by an vacuum arrangement composed by a mechanical pump and a turbomolecular pump which ensures vacuum pressures up to 10^{-7} mbar. The voltage source has a maximal DC voltage of 10 kV. For the detection of the breakdown voltage a voltage slope about 10 V/s is applied. The high voltage is applied between two nearest electrodes so as to get the closest contact gap for the testing. The vacuum chamber has a glass window through which I could see the surface of the trap inside the chamber. A CCD camera is

aligned and connected to a TV monitor. In this manner, I was able to observe directly and in real time when the electrodes broke down. Prior to start to apply the high voltage I verify that there was no previous contact between electrodes to be tested by measuring the possible resistance with the help of a standard multimeter. The breakdown voltage is taken when a intense flash is observed. A statistic of the breakdown voltage is carried out and an average is obtained.

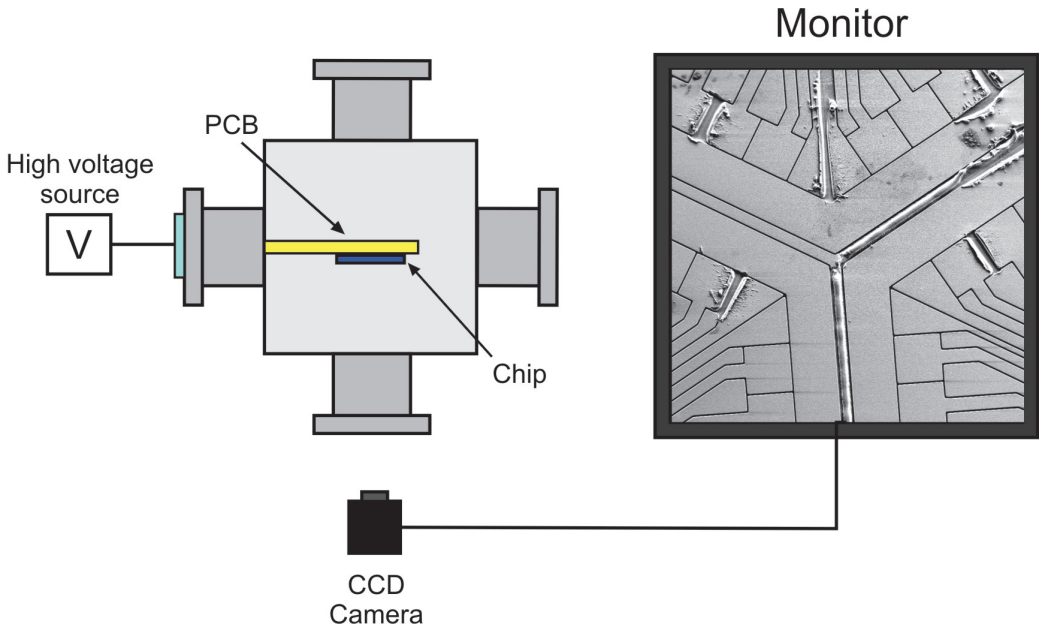


Figure 5.1: Setup for a real-time electrical breakdown test

I placed the Chip 3, which has an inter-electrode gap of 1.2 μm, into the breakdown voltage test setup. A total of eleven pairs of electrodes were tested and I observed that the minimum voltage this trap could stand was 60 V at 1.60×10^{-6} mbar, and the maximal voltage was 240 V at 2.20×10^{-6} mbar. The average breakdown voltage was 180 V with a standard deviation of 56.2 V.

The results from Chip 3 suggested that an increment of the inter-electrode gap of the Au plated electrodes had to be done. Thus I fabricated a new trap having a larger inter-electrode gap[1] of 3.8 μm, labeled Chip 5, and placed into the electrical breakdown setup for testing. The gaps in Chip 5 present an undercut

[1] measured at the bottom of Au plated electrodes

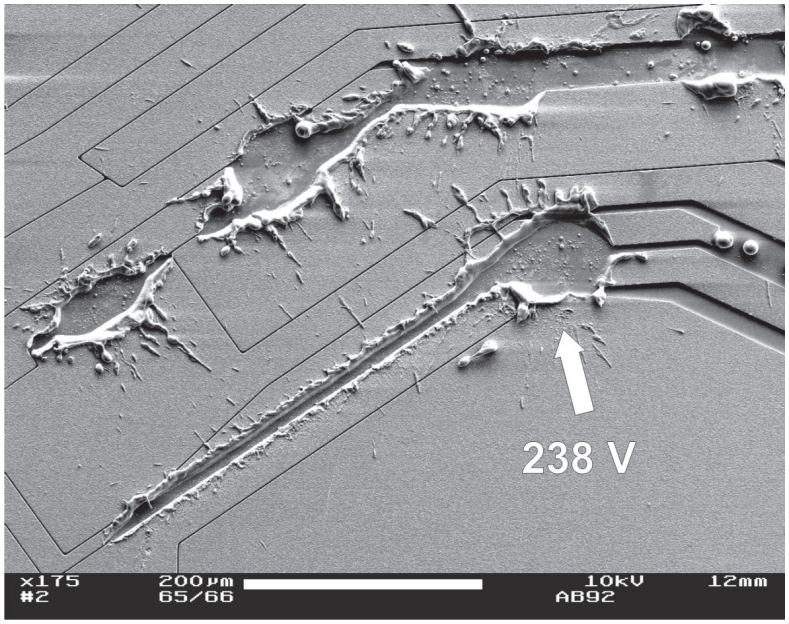


Figure 5.2: SEM picture showing the damage zone on a pair of electrodes, from Chip 3, that stood a breakdown voltage of 238 V

where gap on top of inter-electrode space has a value of 5.36 μm as measured from SEM micrograph in Figure 5.5.

After proper bonding to the chip carrier I placed Chip 5 into the breakdown voltage test setup. For this chip more than 18 pairs of electrode were measured. The minimum breakdown voltage detected was 530 V at 1.3×10^{-6} mbar and a maximum value of 900 V at 5.9×10^{-7} mbar. The average breakdown voltage was 720 V with a standard deviation of 104.2 V. During this testing three different values of the vacuum pressure were utilized in order to see whether it has an influence on the breakdown outcomes. A logarithmic plot of the breakdown voltage against vacuum pressure is presented in Figure 5.6. It is observed, beyond the high values regarding the deviation, that there is a tendency of an improvement of the breakdown voltage when better vacuum pressures are reached. These results, in addition to the average breakdown voltage, suggested that this inter-electrode gap of 3.8 μm is a good candidate for building a surface-electrode for trapping conditions.

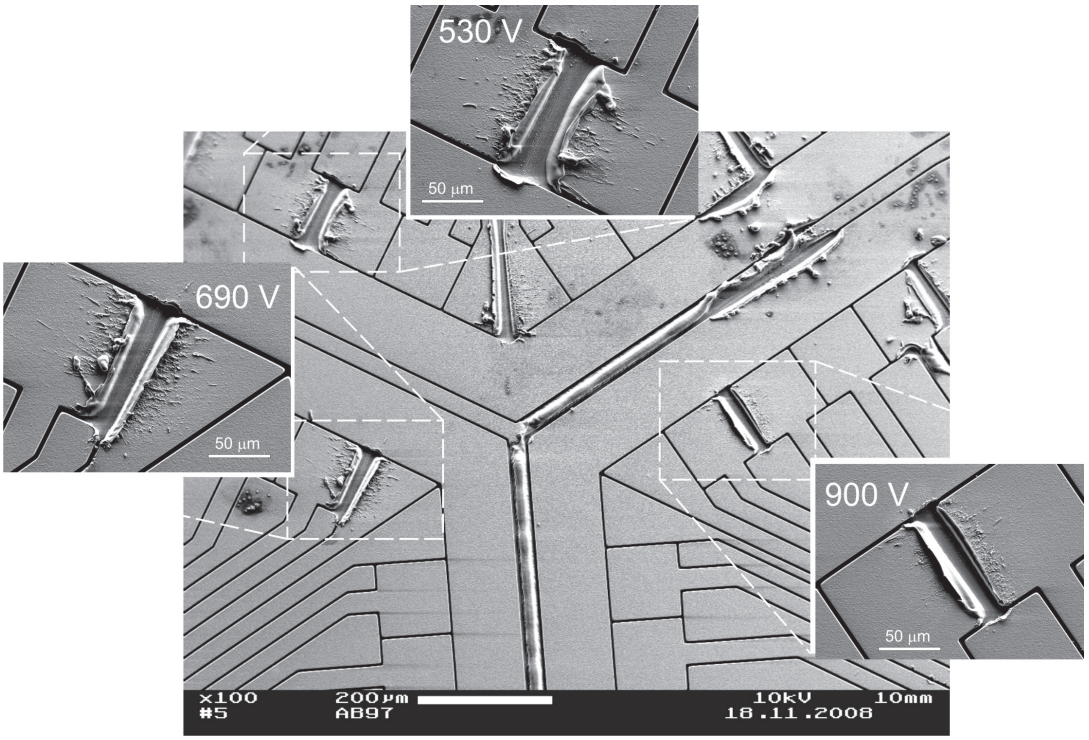


Figure 5.3: SEM micrograph depicts different damaging zones in the center of the trap caused by breakdown voltage. Due to the high electrical discharge the region where the discharge occurs is widened because of fusion of the gold electrodes. The highest breakdown voltage observed in this chip corresponds to a value of 900 V at 5.9×10^{-7} mbar. On the other hand, the lowest breakdown voltage was observed when a value of 530 V at 1.3×10^{-6} mbar was reached.

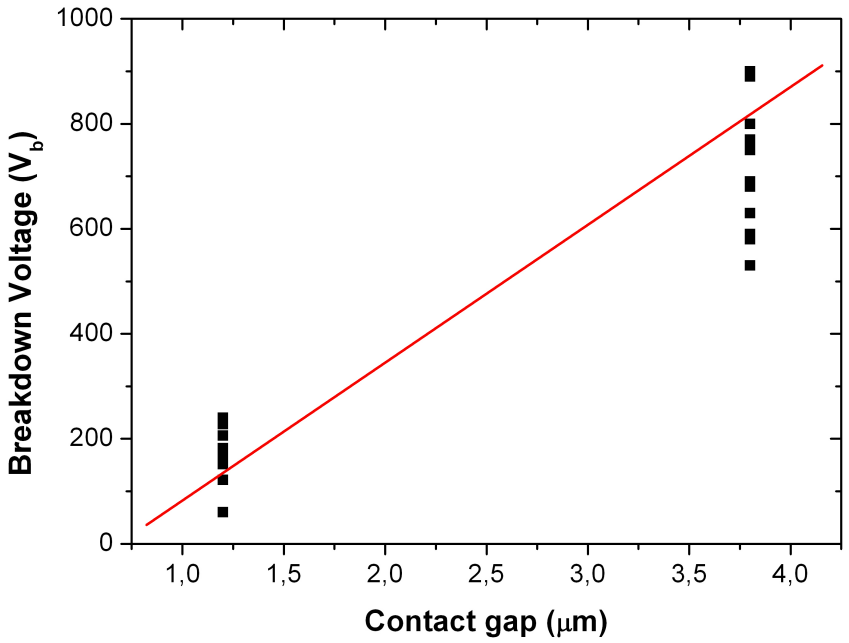


Figure 5.4: It is seen that for a larger gap such as 3.8 μm the breakdown voltage is 720 V.

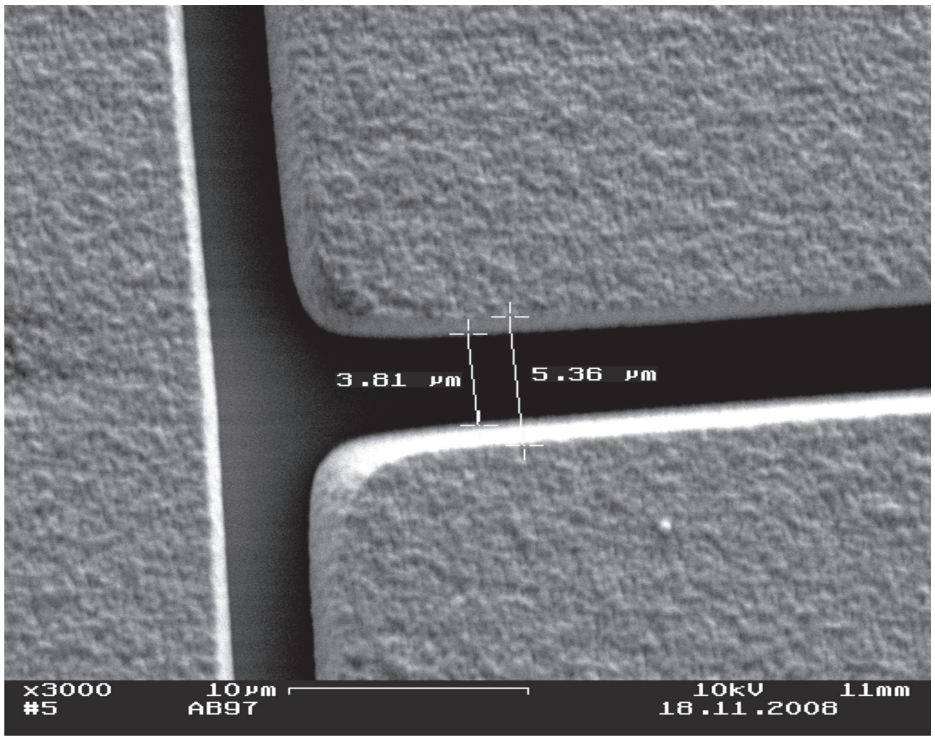


Figure 5.5: SEM image showing the undercut profile achieved in Chip 5. The distance measured at the bottom corresponds to 3.8 μ m and on top to 5.3 μm. From image it also is visible that the sidewalls of Au plated electrodes are smoother when compared to top surface. This smooth sidewalls enhance the expected breakdown voltages value.

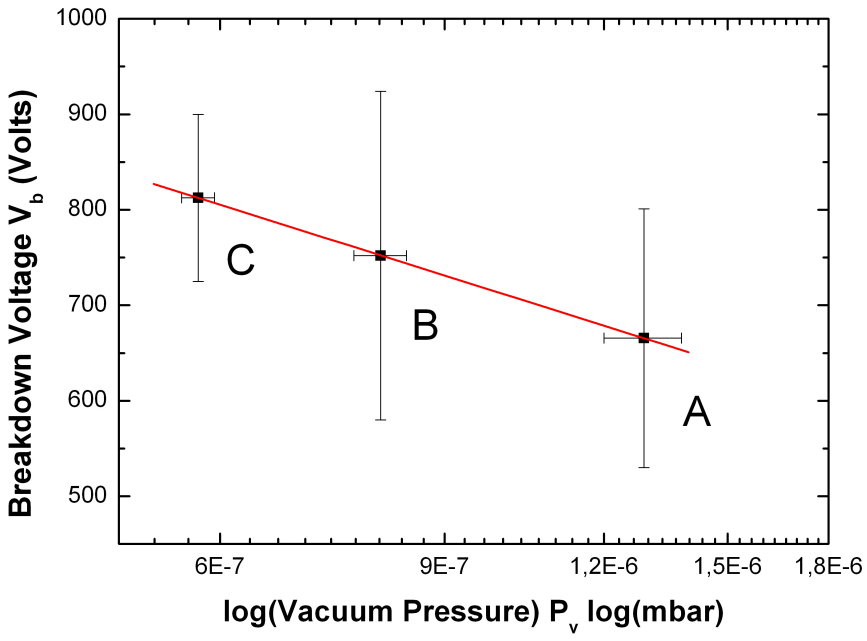


Figure 5.6: Three different vacuum regimes are plotted and it is observed that, in the case of C, a visible improvement of the breakdown voltage is attained. The large errors resulted from the breakdown voltages might be caused by the presence of dirt particles, residues of sputtered gold after breakdown discharge, narrower contact gaps, among others.

Chapter 6

Conclusions

Throughout this master thesis work I have shown a thriving fabrication outline for the construction of a surface-electrode ion trap with the help of conventional microfabrication methods such as photolithography, electroplating and wet etching. Step by step, each fabrication stage, since the substrate cleaning treatment until handling and storage of chip, have been carefully managed to achieve our desired device.

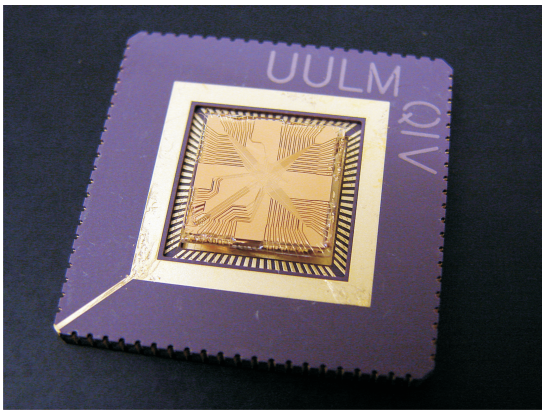


Figure 6.1: Surface-electrode ion trap with an aspect ratio 3:2.

The earlier problems of dirt on glass have been solved by implementing an *unusual* but effective wafer cleaning process as the spin-coater method did. Moreover, I have attained high aspect ratio ≈ 3 for photolithographic patterned features which allow the final acquisition of a high aspect ratio up to 3:2 for the plated gold electrodes. Here, the smallest inter-electrode gap, so far reported for a surface-electrode trap, has been attained with a value of $1.2\,\mu$m, Chip 3.

The Chip 3 and Chip 5 are sustained to electrical breakdown measurements in DC mode. The Chip 3 revealed an average electrical breakdown voltage of 182.3 V. In a similar way, the corresponding average electrical breakdown voltage

for the Chip 5 presented a value of 771 V.

A final chip, Chip 6, has been accomplished with an aspect ratio of 3:2 with an inter-electrode gap of 4.8 μm. The Chip 6 has been assembled and placed into an ultra high-vacuum chamber and prepared for ion trapping.

The fascinating outcomes resulting from the fabrication of the QIV surface-electrode trap (QIV Ulm Chip), as it has been named, opens up the possibility to push further in the microfabrication of planar trap devices. It also has positive repercussions in the attempts for a scalable quantum computer since Y-junctions are expected to bring more benefits for the transport of qubits.

In the near future, it is expected the optimization of the surface-electrode design. In this respect, we will have plenty of room, due to the high-quality properties that AZ® nLOF 2070 for lift-off process has. The same fabrication procedure is expected to be implemented with the exception that gold plated electrodes will be substituted by an evaporated $YBa_2Cu_3O_7$ or NbN layer (35). A more ambitious project scopes the consecution of a surface-electrode trap which be design in such a way that by reducing the width of electrode induces a reduction of the trap depth. This interesting trapping device could address the ions trapped into the nanometer regime, by coupling a surface-electrode ion trap to nanomechanical systems.

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References

[1] Cirac, J. I. and Zoller, P. *Phys. Rev. Lett.* **74**(20), 4091–4094 May (1995). ix

[2] DiVincenzo, D. P. *Scalable Quantum Computers*. Wiley-VCH, Berlin, (2001). ix

[3] Monroe, C., Meekhof, D. M., King, B. E., Jefferts, S. R., Itano, W. M., Wineland, D. J., and Gould, P. *Phys. Rev. Lett.* **75**(22), 4011–4014 Nov (1995). ix

[4] King, B. E., Wood, C. S., Myatt, C. J., Turchette, Q. A., Leibfried, D., Itano, W. M., Monroe, C., and Wineland, D. J. *Phys. Rev. Lett.* **81**(7), 1525–1528 Aug (1998). ix

[5] Roos, C., Zeiger, T., Rohde, H., Nägerl, H. C., Eschner, J., Leibfried, D., Schmidt-Kaler, F., and Blatt, R. *Phys. Rev. Lett.* **83**(23), 4713–4716 Dec (1999). ix

[6] Monroe, C., Meekhof, D. M., King, B. E., Itano, W. M., and Wineland, D. J. *Phys. Rev. Lett.* **75**(25), 4714–4717 Dec (1995). ix

[7] Sackett, C. A., Kielpinski, D., King, B. E., Langer, C., Meyer, V., Myatt, C. J., Rowe, M., Turchette, Q. A., Itano, W. M., Wineland, D. J., and Monroe, C. *Nature* **404**, 256–259 (2000). ix

[8] Nägerl, H. C., Leibfried, D., Rohde, H., Thalhammer, G., Eschner, J., Schmidt-Kaler, F., and Blatt, R. *Phys. Rev. A* **60**(1), 145–148 Jul (1999). ix

[9] Blatt, R. and Zoller, P. *Eur. J. Phys.* **9**, 250–256 (1988). ix

[10] Rowe, M. A., Kielpinski, D., Meyer, V., Sackett, C. A., Itano, W. M., Monroe, C., and Wineland, D. J. *Nature* **409**, 791–794 (2001). ix

[11] Cirac, J. I. and Zoller, P. *Nature* **404**, 579–581 April (2000). ix

[12] Madsen, M. J., Hensinger, W. K., Stick, D., Rabchuk, J., and Monroe, C. *Appl. Phys. B* **78**, 639–651 (2004). ix

[13] Stick, D., Heinsinger, W. K., Olmschenk, S., Madsen, M. J., Schwab, K., and Monroe, C. *Nature Phys.* **2**, 34–39 (2005). ix

[14] Chiaverini, J., Blakestad, R. B., Britton, J., Jost, J. D., Langer, C., Leibfried, D., Ozeri, R., and Wineland, D. J. *Quant. Inf. Comput.* **5**(6), 419–439 (2005). x, 6, 7, 8, 26

[15] Reichle, R., Leibfried, D., Blakestad, R. B., Britton, J., Jost, J. D., Knill, E., Langer, C., Ozeri, R., Seidelin, S., and Wineland, D. J. *Fortschr. Phys.* **54**(8-10), 666–685 (2006). x, 8, 10

[16] Hensinger, W. K., Olschenk, S., Stick, D., Hucul, D., Yeo, M., Acton, M., Deslauries, L., Monroe, C., and Rabchuk, J. *Appl. Phys. Lett.* **88**, 034101 (2006). x

[17] Reichle, R., Seidelin, S., Chiaverini, J., Blakestad, R. B., Bollinger, J. J., Britton, J., Epstein, R., Hume, D., Itano, W. M., Jost, J. D., Knill, E., Langer, C., Leibfried, D., Ozeri, R., Wesenberg, J., and Wineland, D. J. *Poster at NIST workshop on trapped ion quantum computing* (2006). x, 8

[18] Seidelin, S., Chiaverini, J., Reichle, R., Bollinger, J. J., adn J. Britton, D. L., Wesenberg, J. H., Blakestad, R. B., Epstein, R., Hume, D. B., Itano, W. M., Jost, J. D., Langer, C., Ozeri, R., Shiga, N., and Wineland, D. J. *Phys. Rev. Lett.* **96**, 253003 (2006). x, 24

[19] House, M. G. *Phys. Rev. A* **78**, 033402 (2008). x, 8, 9, 10

[20] Paul, W. *Rev. Mod. Phys.* **62**(3), 531–540 (1990). 2, 3

[21] Major, F. G., Gheorghe, V. N., and Werth, G. *Charged Particles Traps: Physics and Techniques of Charged Particles Field Confinement*, volume 37. Springer Series: Atomic, Optical, and Plasma Physics, Heildelberg?, (2005). 3

[22] Ziesel, F. *Spektroskopie und Transport von Ionen in einer Mikrofalle.* (2008). 5, 6

[23] Pearson, C., Leibrandt, D. R., Bakr, W. S., Mallard, W. J., Brown, K. R., and Chuang, I. L. *Phys. Rev. A* **73**, 032307 (2006). 6, 8

[24] Wesenberg, J. H. *Phys. Rev. A* , arXiv:0808.1623v1[quant–ph] (2008). 8

[25] Koch, C. and Rinke, T. J. *Lithography: Theory and Application of Photoresists, Developers, Solvents and Etchants.* Microchemicals, Washington, D. C., (2008/2009). 12, 13, 14, 21, 26, 33, 39, 40, 41, 43, 44, 57, 64

[26] Cherry, O. Master's thesis, University of Waterloo, (2007). 13, 14, 18, 20, 21, 68

[27] Thompson, L. F., Willson, C. G., and Bowden, M. J. *Introduction to Microlithography.* American Chemical Society, Washington, D. C., 2nd edition, (2005). 13

[28] *BOROFLOAT® 33 Datasheet.* SCHOTT®. 15, 26, 30

[29] *http://www.pkl.co.kr/english/product/product05.html.* 17

[30] Madou, M. J. *Fundamentals of Microfabrication: The Science of Miniaturization.* CRC Press, Boca Raton, Florida, 2nd edition, (2002). 22

[31] Labaziewicz, J., Ge, Y., Antohi, P., Leibrandt, D., Brown, K. R., and Chuang, I. L. *Phys. Rev. Lett.* **100**, 013001 (2008). 26

[32] Koukharenko, E., Kraft, M., Ensell, G. J., and Hollinshead, N. *J. Mater. Sci. Electron.* **16**, 741–747 (2005). 27

[33] Kukharenka, E., Farooqui, M. M., Grigore, L., and Kraft, M. *J. Micromech. Microeng.* **13**, S67–S74 (2003). 27

[34] Nagale, M. P. and Fritsch, I. *Anal. Chem.* **70**, 2908–2913 (1998). 36

[35] Kemmler, M., Gurlich, C., Sterck, A., Pohler, H., Neuhaus, M., Siegel, M., Kleiner, R., and Koelle, D. *Phys. Rev. Lett.* **97**(14), 147003 (2006). 78